

Experimental Investigation of Semiconductor Losses in Cryogenic DC-DC Converters

by

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Abstract

As high-temperature superconductor technology approaches commercial applications, for example superconducting magnetic energy storage, superconducting fault current limiters, and superconducting rotary machines for marine propulsion, it is timely to consider the possibility of integrating the associated control equipment into the cryostat with the superconductor. This may bring benefits in terms of the performance of the power electronics or may enable other system benefits such as higher voltage lower current feedthroughs which reduce heat leakage into the cryostat.

This Thesis studies the performance of several DC-DC power conversion techniques at temperatures down to 20 K. In particular hard switching, synchronous rectifier, zero-voltage-switching and multi-level circuit prototypes are examined, focusing on the losses in the semiconductor devices. The prototypes operated from 120 V and 500 V DC supplies at power levels up to 500 W using MOSFET devices and ultrafast, Schottky and silicon carbide diodes. The semiconductors were all in commercial TO220 packages.

Although MOSFET on-state resistance was found to drop by a factor of approximately six at cryogenic temperatures, the device switching speed and switching losses were relatively insensitive to temperature. The diode on-state voltage increased by 20-30 % at low temperatures whilst reverse recovery and the associated losses decreased by a factor of up to ten. The total semiconductor losses in all prototypes reduced at low temperatures, typically exhibiting a minimum value in the region of 50-100 K.

The performance of the hard switching and synchronous rectifier circuits was limited at cryogenic temperatures by switching losses, even though the dead time in the synchronous rectifier was adjusted to compensate for the increase in MOSFET gate threshold voltage at

low temperatures. The zero-voltage-switching prototype offered the largest reduction in semiconductor losses at low temperatures, the losses were reduced to 18 % of the room temperature value. Furthermore, since the remaining losses were almost entirely due to MOSFET conduction, further reductions could be easily achieved by paralleling additional devices. The performance of the multi-level circuits was limited by switching losses and the large number of series connected devices; however, a zero-voltage-switching synchronous rectifier variant of the circuit was suggested to overcome some of these limitations.

To my parents.

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List of abbreviations and symbols

Abbreviation	Complete forms
2G	2nd Generation
BJT	Bipolar Junction Transistor
BSCCO	Bismuth Strontium Calcium Copper Oxide
COTS	Commercial Off The Shelf
CPE	Cryogenic Power Electronics
D-SMES	Distributed Superconducting Magnetic Energy Storage
FCL	Fault Current Limiter
HTS	High Temperature Superconductor
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
LTS	Low Temperature Superconductor
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPP	Molypermalloy Powder
MRI	Magnetic Resonance Imaging
NbTi	Niobium Titanium
Nb ₃ Sn	Niobium Stannide
NMI	Nuclear Magnetic Imaging
NPT	Non Punch Through
n^-	Low doped n region
n^+	Highly doped n region
p^+	Highly doped p region
PCB	Printed Circuit Board
PCS	Power Conditioning System
PT	Punch Through
PWM	Pulse Width Modulation
PFM	Pulse Frequency Modulation
SCG	Superconducting Generator
SiC	Silicon carbide
SiGe	Silicon Germanium
SMES	Superconducting Magnetic Energy Storage
YBCO	Yttrium Barium Copper Oxide
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVS-CV	Zero Voltage Switching Clamped Voltage

Symbol	Description	Unit
C_{In}	Input capacitor in the two-level converters	F
C_{In1}	Input capacitor in the three-level converters	F
C_{In2}	Input capacitor in the three-level converters	F
C_O	Output capacitor	F
$C_{D'S'}$	MOSFET drain-source capacitance	F
C_{GD}	MOSFET gate-drain capacitance (Miller capacitance)	F
$C_{G'D'}$	MOSFET gate-drain capacitance when $v_{D'S'} \geq V_T + I_O / g_{fs}$	F
$C_{G'D''}$	MOSFET gate-drain capacitance when $v_{D'S'} < V_T + I_O / g_{fs}$	F
$C_{G'S'}$	MOSFET gate-source capacitance	F
C_{r1}	Snubber capacitor across S_1 in the soft-switching converter	F
C_{r2}	Snubber capacitor across S_2 in the soft-switching converter	F
D	Duty ratio	-
D_1	Freewheeling diode in the single-transistor buck converters	-
D_{C1}	Voltage-clamping diode in the three-level buck converters	-
D_{C2}	Voltage-clamping diode in the three-level buck converters	-
D_{T1}	Freewheeling diode in the three-level buck converters	-
D_{T2}	Freewheeling diode in the three-level buck converters	-
g_{fs}	MOSFET transconductance	S
I_{AV}	Average current through device	A
I_{In}	Input DC current	A
I_{Lmax}	Maximum inductor current	A
I_{Lmin}	Minimum inductor current	A
I_O	Output DC current	A
I_{RMS}	RMS current through device	A
I_{RR}	Diode peak reverse recovery current	A
i_C	Instantaneous current through the capacitor C_{In}	A
i_{CIn1}	Instantaneous current through the capacitor C_{In1}	A
i_D	Instantaneous current through the MOSFET	A
i_L	Instantaneous current through the inductor	A
i_{S1}	Instantaneous current through the MOSFET S_1	A
i_{S2}	Instantaneous current through the MOSFET S_2	A
i_{ST3}	Instantaneous current through the MOSFET S_{T3}	A

J_F	Forward current density	A/cm ²
J_S	Saturation current density	A/cm ²
K	Rate of change of the MOSFET drain-source voltage	V/s
K_1	Rate of decrease of the MOSFET drain-source voltage when $v_{D'S'} \geq V_T + I_O / g_{fs}$	V/s
K_2	Rate of decrease of the MOSFET drain-source voltage when $v_{D'S'} < V_T + I_O / g_{fs}$	V/s
K_3	Rate of increase of the MOSFET drain-source voltage when $v_{D'S'} < V_T + I_O / g_{fs}$	V/s
K_4	Rate of increase of the MOSFET drain-source voltage when $v_{D'S'} \geq V_T + I_O / g_{fs}$	V/s
K_L	Ratio of inductor AC current ripple over DC current	
k	Boltzmann's constant	J/K
L	Filter inductor in the buck converter	H
L_D	MOSFET drain lead inductance	H
L_S	MOSFET source lead inductance	H
P_{Cond_Diode}	Diode conduction loss	W
P_{Cond_MOSFET}	MOSFET conduction loss	W
Q_r	Diode reverse recovery charge	C
q	Electric charge of an electron	C
R	Load resistance	Ohm
$R_{DS(on)}$	MOSFET on-state resistance	Ohm
R_D	Drift region resistance in a Schottky diode	Ohm
R_G	MOSFET gate resistance	Ohm
$R_{G'}$	MOSFET polycrystalline silicon gate resistance	Ohm
R_{S+C}	Substrate and ohmic contact resistance in a Schottky diode	Ohm
S_1	Power MOSFET in the buck converters	-
S_2	Power MOSFET in the synchronous rectifiers	-
S_{C1}	Voltage-clamping MOSFET in the three-level ZVS buck converters	-
S_{C2}	Voltage-clamping MOSFET in the three-level ZVS buck converters	-
S_{T1}	Power MOSFET in the three-level buck converters	-
S_{T2}	Power MOSFET in the three-level buck converters	-
S_{T3}	Power MOSFET in the three-level buck converters	-
S_{T4}	Power MOSFET in the three-level buck converters	-
T	Operating temperature	K
T_1	Time interval for the S_1 gate-source voltage to decrease from the plateau voltage to V_T	s

T_2	Time interval for the S_1 gate-source voltage to decrease from V_T to zero	s
T_3	Time interval for the S_2 gate-source voltage to increase from zero to V_T	s
T_4	Time interval for the S_2 gate-source voltage to increase from V_T to the plateau voltage	s
T_5	Time interval for the S_2 gate-source voltage to decrease from the plateau voltage to V_T	s
T_6	Time interval for the S_2 gate-source voltage to decrease from V_T to zero	s
T_7	Time interval for the S_1 gate-source voltage to increase from zero to V_T	s
T_8	Time interval for the S_1 gate-source voltage to increase from V_T to the plateau voltage	s
T_{Dead}	Fixed dead time in the synchronous rectifier	s
T_S	Switching period	s
t_0	The instant when the diode forward current drops to zero	s
t_1	The instant when the diode reverse recovery current is maximum	s
t_2	The instant when the diode reverse recovery current falls to zero	s
t_b	The blanking time in the soft-switching converter	s
t_{rr}	Diode reverse recovery time	s
V_B	Metal-semiconductor barrier voltage drop	V
V_{BR}	Breakdown voltage	V
V_{D^*}	MOSFET drain-source voltage at the end of t_1	V
V_{DD}	Power supply DC voltage during the MOSFET transient analysis	V
V_F	Forward voltage drop of the power diode at rated current	V
V_{GH}	High level of the MOSFET gate drive voltage	V
V_{In}	Input DC voltage	V
V_O	Output DC voltage	V
V_R	Voltage drop across the resistive region in a Schottky diode	V
V_T	MOSFET threshold voltage	V
V_{ab}	H-bridge output voltage	V
v_{CIn1}	Instantaneous voltage across C_{In1}	V
$v_{D'S'}$	Instantaneous MOSFET drain-source voltage	V
v_F	Instantaneous diode on-state voltage	V
v_{GG}	Instantaneous MOSFET gate drive voltage	V
$v_{G'S'}$	Instantaneous MOSFET gate-source voltage	V
v_{In}	Instantaneous input voltage	V

v_L	Instantaneous voltage across the filter inductor	V
v_O	Instantaneous voltage across the output capacitor	V
v_{GS1}	Instantaneous S_1 gate-source voltage	V
v_{GS2}	Instantaneous S_2 gate-source voltage	V
v_{S1}	Instantaneous S_1 drain-source voltage	V
v_{S2}	Instantaneous S_2 drain-source voltage	V
v_{ab}	Instantaneous H-bridge output voltage	V
ΔI_L	Peak-to-peak inductor current ripple	A
ΔV_{In}	Peak-to-peak input voltage ripple	V
ΔV_O	Peak-to-peak output voltage ripple	V
t_1	Time interval for the drain current transition during the MOSFET turn-on	s
t_2	Time interval for the drain-source voltage transition during the MOSFET turn-on	s
t_3	Time interval for the gate-source voltage to increase from the plateau voltage to V_{GH} during the MOSFET turn-on	s
t_4	Time interval for the gate-source voltage to decrease from V_{GH} to the plateau voltage during the MOSFET turn-off	s
t_5	Time interval for the drain-source voltage transition during the MOSFET turn-off	s
t_6	Time interval for the drain current transition during the MOSFET turn-off	s
t_7	Time interval for the gate-source voltage to decreases from V_T to zero during the MOSFET turn-off	s
t_D	Time delay for MOSFET turn-on	s
t_G	Time constant $t_G = (R_G + R_{G'}) (C_{G'S'} + C_{G'D'})$	s
$t_{G'}$	Time constant $t_{G'} = C_{G'D'} (R_G + R_{G'})$	s
t_m	Time constant $t_m = g_{fs} L_D$	s

Chapter 1

Introduction and literature review

1.1 Introduction

Superconductivity was first discovered in 1911 [1-1]; however the extreme cryogenic environment that was required limited the development of applications until the late 1980s when the discovery of high temperature superconductors [1-2, 1-3] stimulated much more rapid progress. The original low temperature superconductors, such as niobium-titanium (NbTi), require expensive refrigeration systems to operate below their critical temperatures of around 4.2 K [1-4]. The development of high temperature superconductors (HTS) has made superconductivity possible at much higher temperatures allowing the use of simpler, less costly and more efficient refrigeration systems. Furthermore higher current densities and magnetic fields can be accommodated. The HTS wires, bismuth-strontium-calcium-copper-oxide (BSCCO) and yttrium-barium-copper-oxide (YBCO) with critical temperatures of 110 K and 93 K respectively, have thermally and mechanically stable properties with high critical current levels and have made superconducting devices easier to realise [1-5, 1-6].

Applications are now emerging in a broad range of areas where the properties of superconductors offer the possibility of making significant performance gains. For example in medical imaging where superconducting coils are used to produce the high magnetic fields required for NMI systems and in communications where superconducting circuits are used to make filters with very high Q factor. In the area of electrical power engineering the

use of superconductors allows much higher current densities to be achieved and conduction losses to be virtually eliminated, enabling reductions in equipment size and weight, or increases in power throughput for the same size. The main superconducting power applications are summarised in Section 1.2.

As superconducting power applications are developed the possibility arises of co-locating any associated power electronics equipment in the cryo-system with the superconductor, potentially improving the performance of the power electronics itself, or bringing other system level benefits. Although a significant amount of work has been published on the characteristics of standard power electronic devices at low temperatures, particularly on-state and breakdown voltages, comparatively little has been reported on the overall performance of complete converters. This Thesis therefore seeks to examine practically the operation and performance of several DC-DC converter topologies, in particular looking at the semiconductor performance, and to identify the most appropriate and effective circuit techniques. The published work on the cryogenic operation of power electronics is reviewed in Section 1.3.

1.2 Superconducting power applications

As new superconducting materials continue to be developed and the cost of manufacture continues to reduce, large scale applications are starting to appear in areas, such as electrical power systems, transport and rotary machines [1-7, 1-8, 1-9]. These include superconducting transmission lines, superconducting generators and transformers, superconducting magnet energy storage, fault current limiters, superconducting motors and magnetic levitation of trains. These applications will be briefly reviewed in the following sections.

1.2.1 Superconducting transmission lines

Superconducting power cables can carry three to five times more power and provide higher system efficiency than conventional copper cables of similar size [1-9].

One of the first demonstrations, a 1000 MVA system was constructed utilising low temperature superconductors, Niobium Stannide (Nb_3Sn), in flexible cables 2×115 m at 9 K and operated from 1982 to 1986 confirming the technical feasibility [1-10]. However, numerous superconducting power transmission projects including this one were cancelled for cost reasons [1-7, 1-10, 1-11].

More recently there has been renewed interest using HTS materials with critical temperatures of around 110 K and liquid nitrogen cooling (77 K) [1-7, 1-9, 1-11, 1-12]. For example a 3 kA, 13.2 kV AC transmission line of 200 m length was commissioned in 2006, developed jointly by Southwire and NKT Cables, which can carry as much current as 18 large copper cables and approximately three times more current than other superconducting transmission systems that are operational or under construction [1-13, 1-14].

1.2.2 Superconducting generators and transformers

Numerous papers describe synchronous generators which use superconducting DC field windings, allowing higher current densities to be used which result in higher magnetic fields and a more efficient and smaller machine [1-7, 1-8, 1-9, 1-15, 1-16, 1-17]. For example General Electric (GE) built a 100 MVA HTS superconducting generator for civil use [1-17], but the project was abandoned in 2006 due to economic and technical reasons [1-18]. However, several military programmes continued to pursue the technology to increase power density for applications where space or weight is restricted, such as ships and aircraft [1-18, 1-19]. It is estimated that a 5 MW generator using YBCO could be more than ten times lighter than a conventional generator [1-9, 1-19].

It is claimed in [1-7] that a superconducting power transformer would have half the size and weight of a conventional device, furthermore the fire and environmental hazards associated with the cooling oil in conventional transformers would be eliminated. In addition the life expectancy would be increased [1-7, 1-9]. In 2003 Waukesha Electric Systems and IGC SuperPower built and tested a 5/10 MVA 3-phase HTS transformer with primary/secondary voltage ratings of 24.9 kV/4.2 kV. This was the second phase of a three-stage programme which aims to build a 30/60 MVA unit in the final phase [1-21].

1.2.3 Superconducting magnet energy storage (SMES)

Superconducting magnet energy storage (SMES) systems store energy in the magnetic field of a superconducting DC inductor, and are now commercially available offering flexible, reliable, and fast-acting power compensation to electrical power systems [1-22]. SMES systems may be used to suppress voltage sags and swells or for load levelling. Due to its rapid response (MW/milli-seconds), it is claimed that the SMES system described in [1-23] has the potential to improve power transmission stability, frequency control, sensitive load protection and power quality at power and energy levels of 20-200 MW and 50-500 MJ. American Superconductor's D-SMES (Distributed Superconductor Magnetic Energy Storage) system is a mobile device that can be easily located exactly where voltage mitigation is needed in the network, providing up to 3 MW of instantaneous real power from the superconductor magnet and up to 8 MVAR reactive power [1-24]. SMES systems require extensive power conditioning circuits including AC-DC and DC-DC converters and filter components. The source of power losses in SMES systems is primarily from the power conditioning circuits [1-25].

1.2.4 Fault current limiters

Fault current limiters (FCL) using high temperature superconductors have been explored since the late eighties [1-26 to 1-31]. These devices limit the fault current to a desired level by inserting impedance into the circuit, whereas they stay in the superconducting state with

no resistance when there is no fault [1-31]. Fault current limiters can reduce voltage transients during fault conditions and enable smaller, lower-rated switch gear to interrupt the fault [1-29, 1-30, 1-31]. Ref [1-32] describes a FCL based on American Superconductor's 2G HTS wire for distribution and transmission voltages up to 138 kV AC. The device limits the fault currents to 3-5 times the rated current [1-32].

1.2.5 HTS Motors

The initial applications for HTS motors are likely to be in transport, particularly for naval and commercial ship electric propulsion, where critical size and weight savings will increase the design flexibility [1-33, 1-34]. Typically superconducting machines, employing superconducting field windings, are much more compact and lighter than conventional machines [1-35, 1-36, 1-37]. Advances in rotor design make a superconducting motor around one-third the size and one-half the weight of a conventional motor with the same power ratings [1-38], and a lower manufacturing cost can be achieved [1-37, 1-38]. Additional benefits of superconducting motors include higher efficiency even at partial load conditions and reduced acoustic noise due to the absence of armature teeth [1-37, 1-38]. A 5 MW, 230 RPM, 6-pole AC synchronous motor was delivered to the U.S. Navy in July 2003 by American Superconductor, employing a high temperature superconducting field winding operating at 32 K on the rotor and a conventional, copper, air-cored winding on the stator [1-37]. Furthermore the company completed factory testing of a 36.5 MW HTS marine propulsion motor in March 2007 and was making preparations for the next testing phase [1-39].

1.2.6 Magnetically levitated trains

The superconducting, magnetically levitated train that was tested in Japan on December 2 2003 is another example of the use of superconductor technology. The train achieved a new record speed of 581 km/h [1-40]. The superconducting coils, used in the prototype trains, were made of low temperature superconductor NbTi, which requires complex cooling systems to maintain the operating temperature of 4 K. Research and development

programmes are under way to use high temperature superconducting wires in future magnetically levitated trains [1-40, 1-41].

1.3 Review of cryogenic power electronics

The operation of power semiconductor devices and circuits at low temperatures has received increasing attention as superconducting power applications have been developed. The cryogenic operation of power semiconductor devices can result in improved switching speed and lower on-state voltage than at room temperature. Particularly large benefits have been reported for majority carrier devices like MOSFETs operating at around 77 K, liquid nitrogen temperature [1-42, 1-43]. It has also been demonstrated that operation at low temperatures could provide other benefits, such as reduced package volume, higher current densities and increased reliability [1-25, 1-44, 1-45]. Several recent studies have concluded that there is a great potential for cryogenic power conversion in future military systems, such as propulsion motors and power generators on board ships and aircraft, where size and weight are the primary design considerations [1-46, 1-47].

This section will review the published work on the cryogenic performance of silicon power semiconductor devices, followed by germanium and silicon germanium devices. Research on the cryogenic behaviour of power conversion circuits is also summarised.

1.3.1 Schottky barrier diode

A Schottky barrier diode, Figure 1-1, consists of a thin film of metal in direct contact with a semiconductor. The metal film is usually deposited on an n -type semiconductor, referred to as a metal-semiconductor rectifying contact, and an n -drift region is added to withstand the reverse voltage. The forward voltage V_F consists of two parts, the metal-semiconductor barrier voltage drop V_B and the voltage drop across the resistive region V_R as shown in (1-1).

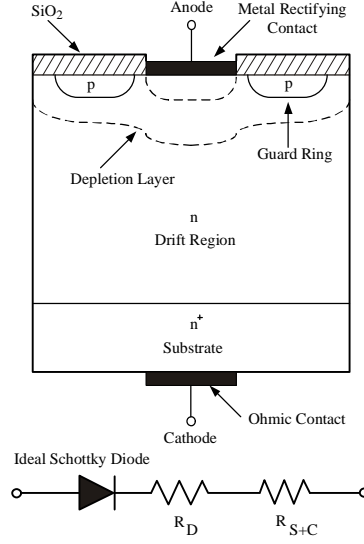


Figure 1-1 Schottky barrier diode structure and equivalent circuit

$$V_F = V_B + V_R \quad (1-1)$$

$$V_F = \frac{kT}{q} \ln\left(\frac{J_F}{J_S}\right) + R_D J_F \quad (1-2)$$

k is the Boltzmann constant, T is the operating temperature, q is the electron charge, J_F is the forward current density, J_S is the saturation current density and R_D is the specific resistance of the voltage blocking drift region, while the resistance of the n^+ substrate and ohmic contact, R_{S+C} , is normally negligible [1-25].

At high current densities, the dominant temperature effect on the forward voltage arises from the electron mobility in the drift region. The reduction in temperature leads to a dramatic decrease in the ohmic portion of the on-state voltage drop. The metal-semiconductor voltage drop faces two competing effects as temperature falls from 300 K to 77 K, a decline in kT/q tending to reduce its value and a reduction in the saturation current density J_S tending to increase its value. The net effect is an increase in the metal-semiconductor voltage drop with a decrease in temperature [1-25]. Therefore, the Schottky diode forward voltage

may exhibit a positive or negative temperature coefficient at different temperatures and different currents, depending on the relative sizes of the two voltage components.

The reverse bias characteristic of a Schottky diode is determined by the spreading of the space charge region into the n -type region. With a Schottky contact of finite area the breakdown voltage is limited to less than 100 V by the field concentration caused by the curvature of the space charge region at the edge of the contact area [1-48]. This can be improved by using an edge termination technique. The preferred method is the diffused p^+ guard ring shown in Figure 1-1. Although this forms a p - n junction diode in parallel with the Schottky diode, the lower forward voltage of the Schottky junction ensures that the p - n junction is only forward biased sufficiently to inject carriers into the active region under surge conditions [1-48]. This type device is known either as a Schottky P-i-N (SPIN) diode, or as a merged power Schottky (MPS) diode [1-48].

The reduction in temperature results in much lower leakage current during the reverse bias operation of a Schottky diode. Theoretically the ideal breakdown voltage of a silicon Schottky diode is predicted to increase to twice the room temperature value at 77 K [1-25]. However, for MPS/SPIN diodes, under a reverse biased voltage the space charge region expands to shield the Schottky junction from the applied voltage by JFET action resulting from the diffused p^+ regions [1-48]. Therefore the device tends to behave like a p - n junction under reverse bias conditions and the breakdown voltage falls at low temperature.

1.3.2 P-i-N diode

A P-i-N diode, Figure 1-2, consists of a heavily doped p^+ type region, an intrinsic layer, n^- , and a heavily doped n^+ substrate. The n^- layer is not found in low power diodes and is used to absorb the depletion layer of the reverse-biased p - n junction. The thickness depends on the breakdown voltage of the device. Most silicon rectifiers with blocking voltages greater than 200 V are P-i-N diodes [1-25].

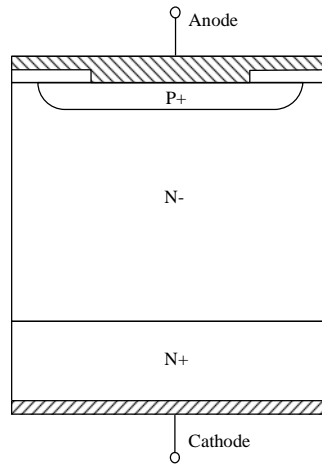


Figure 1-2 P-i-N diode structure

Ref [1-49] reported an experimental study into the behaviour of a 1200 V P-i-N diode over the 77-300 K temperature range. At low current, 4 A, the on-state voltage increased at low temperatures, whereas at high current, 10 A, 2.5 times the rated current, the on-state voltage fell at low temperatures. Also, the reverse recovery waveforms improved at low temperatures; the peak reverse current and recovery time decreased by almost an order of magnitude at 77 K, principally due to the reduction in carrier lifetime [1-49].

It was shown in [1-49] by examination of analytical models that at room temperature the total forward current is dominated by recombination in the mid region of the diode, however, it is dominated by the end region recombination currents at 77 K. It was also explained that the band gap narrowing effect, the increase in diffusion coefficients and the reduction in carrier lifetime should also be considered for a proper understanding of the power P-i-N diode operation at low temperatures. It was concluded that P-i-N diodes can be operated at higher frequencies and higher current densities at cryogenic temperatures as compared to room temperature [1-25, 1-49, 1-50].

1.3.3 Power MOSFET

The power MOSFET has a vertical structure as shown in Figure 1-3. Conduction occurs by majority carriers through an inversion layer that is created in the p body region underneath the insulated gate. The inversion layer is formed by a positive gate-source voltage; the electrical field attracts electrons to the surface of the p -base body region under the gate. Early papers on the cryogenic behaviour of MOSFETs were published in the 1970s [1-42, 1-43], however many more papers have been published since the late 1980s [1-51 to 1-68].

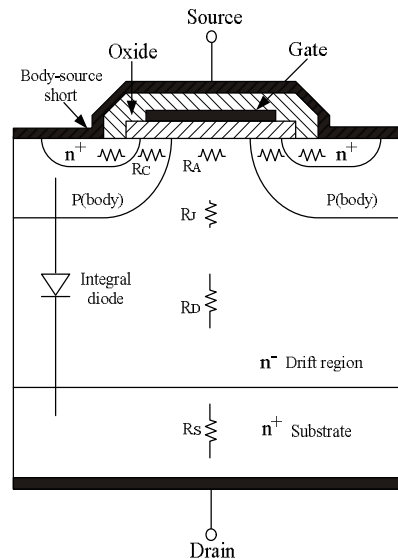


Figure 1-3 N-channel power MOSFET structure

Simple, lumped parameter analytical models for the power MOSFET have been used to explain the device operation at cryogenic temperatures [1-51, 1-61 to 1-64]. The MOSFET on-state resistance is made up by four main components, the resistances of the inversion, accumulation, JFET and drift regions. The relative sizes of these component resistances vary according to the design of the MOSFET. The major contribution to the on-state resistance of higher voltage MOSFETs is from the drift region, whereas the inversion layer tends to be the main contributor to the on-resistance of low voltage MOSFETs. The increase in carrier mobilities at low temperatures in these regions essentially determines the reduction in the MOSFET on-state resistance at low temperatures [1-25, 1-51]. The on-state resistances of

three power MOSFETs with ratings of 50 V, 250 V and 500 V were observed to decrease by 50 %, 85 % and 90 % respectively at 77 K compared to room temperature [1-51].

At extremely low temperatures, typically below 40 K for silicon, the MOSFET on-state resistance tends to increase with further temperature reductions due to only a small number of carriers being available [1-53, 1-65]. This is referred to as carrier freeze-out, and is most significant in the JFET and the drift regions [1-25]. Therefore, the carrier freeze-out phenomenon tends to be much more obvious in higher voltage MOSFETs due to the dominance of the drift region resistance in these devices.

Both MOSFET threshold voltage and transconductance increase at low temperatures. The threshold voltage was reported to increase at 77 K by about one volt compared with room temperature [1-51, 1-52, 1-58], which results from the fall in intrinsic carrier concentration at low temperatures [1-25]. A larger gate-source voltage is needed to form the inversion layer. The increase in transconductance is attributed to the increase in inversion layer mobility at low temperatures [1-25]. The transconductance of the MOSFETs tested in [1-51] was reported to increase by 2-3 times at 77 K.

The breakdown voltage of the power MOSFET decreases at low temperatures, which is determined by the intrinsic *p-n* junction reverse breakdown behaviour. More effective impact ionisation at low temperatures results in avalanche breakdown occurring at reduced voltage levels [1-25, 1-51]. It was reported that the breakdown voltage of six different MOSFETs decreased by 19 – 23 % at 77 K [1-68].

The switching performance of power MOSFETs has been reported to improve at cryogenic temperatures [1-25, 1-51]. The MOSFET switching characteristics in [1-52, 1-57] at high frequency were significantly improved at cryogenic temperatures with a shorter turn-on delay and sharper turn-on and turn-off slopes. The turn-on time of a CoolMOS device was reported to decrease by up to one-third at 83 K, substantially caused by the diminished

reverse recovery charge of the freewheeling diode [1-56]. However, much smaller reductions in the turn-on time were reported in [1-59] at low temperatures. These differences seem to be due to individual characteristics of the devices and also the test circuits that were used. In addition, the reverse current and recovery time of the body diode decrease significantly at low temperatures, for example they reduced by a factor of three to five at 77 K for the MOSFETs tested in [1-54]. These improvements at low temperatures, along with the better thermal conductivity of silicon suggest that the potential exists for efficiency increases and considerable size, weight and cost reductions[1-66 to 1-68].

1.3.4 IGBT

The insulated gate bipolar transistor (IGBT), Figure 1-4, has a similar structure to the MOSFET except for the addition of a p^+ layer beneath the n drift region. This structure may be considered to combine the advantages of a bipolar device and a MOSFET, giving the IGBT a high current handling capability due to the injection of minority carriers (holes) from the p^+ substrate. However the hole injection degrades the IGBT turn-off performance causing a tail current that limits the device's high frequency applications. Presently the IGBT technology is the preferred option for power switching devices with breakdown voltages over 1000 V [1-25].

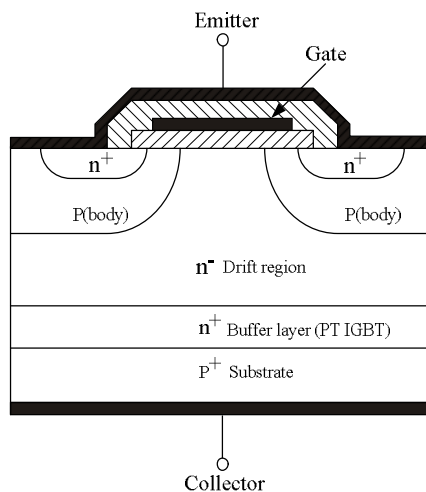


Figure 1-4 N-Channel IGBT structure

The PT (punch-through) and NPT (non-punch-through) IGBTs, also referred to as asymmetrical (with an n buffer layer) and symmetrical (without an n buffer layer) respectively, and the newer, trench gate IGBT, were characterised at low temperatures in terms of their static and dynamic behaviour, and analytical IGBT models were introduced for low temperature operation [1-69 to 1-77].

At low temperatures the reduction in the intrinsic carrier concentration requires a higher voltage level across the gate and emitter of an IGBT to form the inversion layer in the p -base region, resulting in an increased threshold voltage. The measured threshold voltage was found to increase about one volt at 77 K [1-73], and the transconductance was measured to increase by a factor of two at 77 K [1-73], which was attributed to the increase in inversion layer mobility at low temperatures [1-25]. At the rated current, the on-state voltage of an n -channel asymmetric (PT) IGBT was reported to decrease approximately by one-third at 77 K [1-73]. The on-state voltages of the 600 V PT IGBT, 1700 V NPT IGBT and trench IGBT were observed to decrease across the 300-100 K temperature range at 100 A in [1-74 to 1-77], principally due to the significant decrease in the MOSFET component of on-state voltage in the three devices. The breakdown voltage of the PT and NPT IGBT devices decreased approximately by 30 % over the 300-50 K range, whereas the breakdown voltage of the trench IGBT decreased by 60 % which was attributed to the field stop layer in the trench device [1-74 to 1-77]. The switching performance of the IGBT improves at low temperatures; the turn-off time was found to decrease by more than 60 % at 77 K due to the reduction in carrier lifetime [1-25, 1-73].

1.3.5 Germanium and silicon germanium devices

An interesting avenue of research has been to examine the possibility of designing and fabricating devices specifically for cryogenic operation. The use of germanium instead of silicon has been considered since the freeze-out temperature of dopants in germanium is much lower than in silicon, and also the carrier mobility in germanium is higher than that in silicon at low temperatures. Therefore, a Ge diode can operate from room temperature down to 4 K and has lower forward voltage drop than does a silicon part [1-78].

Ge cryogenic power device development has been undertaken by NASA and its collaborators. A Ge power diode with a nominal 10 A forward current has been demonstrated with a breakdown voltage of 400 V at temperatures down to 4 K. Also *p*-channel enhancement Ge metal-insulator-semiconductor field-effect transistors (MISFETs), JFETs and BJTs were fabricated and characterised at temperatures down to 4 K [1-79, 1-80], but their current and voltage ratings were not mentioned.

Power semiconductor devices based on silicon germanium (SiGe) are being developed by GPD Optoelectronics Corp in cooperation with Auburn University, motivated by the NASA deep space exploration programme [1-81]. A 50 V, 5 A SiGe heterojunction bipolar transistor was designed and fabricated, which was examined along with a SiGe diode in a 100 W, 24 V/48 V, 100 kHz boost power converter at low temperatures. The conversion efficiency was reported to increase from 75% at room temperature to 89 % at 30 K [1-81].

1.3.6 Passive components

Cryogenic experiments on commercially available capacitors showed that the effect of low temperature on the capacitor depends essentially on the dielectric medium being used [1-82, 1-83]. Capacitors such as polypropylene, polycarbonate, mica, film and ceramic could operate properly at 77 K, and some capacitors had a decrease in leakage current and dissipation factor at low temperature. It was concluded that further experimental studies were required to fully characterise capacitors for potential cryogenic use [1-82, 1-83].

Magnetic cores were examined for potential applications at cryogenic temperatures [1-84]. Experimental results showed that molypermalloy and high flux core-based inductors exhibited constant inductance against temperature, whereas the inductance of ferrite-cored components decreased by a factor of seven from 25°C to -190°C [1-84]. The paper suggested that more testing was needed to evaluate these cores under long term exposure to low temperatures [1-84].

1.3.7 Integrated circuits

A number of commercial analogue-to-digital converters, oscillators and PWM controllers were evaluated at low temperatures [1-85 to 1-92]. The analogue-to-digital converters were reported to operate well down to -190°C [1-90]; those with an external reference were the most accurate [1-85]. The temperature compensated oscillator that was tested maintained frequency stability down to -189°C [1-85]. Some PWM controllers that were evaluated maintained satisfactory functionality at -190°C [1-91]. However, it was concluded that more comprehensive tests were required to fully characterise the performance of PWM and A/D chips for low temperature space missions [1-90, 1-91].

1.3.8 Commercial power supply modules

Several commercially available DC-DC converter modules were investigated for potential use in future space missions [1-92 to 1-97]. These 3.3 V output modules, ranged in electrical power from 8 W to 13 W, and their input voltages ranged from 9 V to 75 V. The circuits were characterised in terms of the steady-state and dynamic performance with temperature from 20°C to -180°C . The low temperature evaluation included the output voltage regulation, efficiency, input and output current ripple and dynamic behaviour in response to temperature changes. Some modules were found to become unstable in terms of voltage regulation at low temperatures.

1.3.9 Low power, low voltage DC-DC converters

Developments in high temperature superconductivity and low temperature semiconductors have motivated the investigation of power conversion circuits at low temperatures. During the 1990s there has been a surge of activity in the examination of power converters at low temperature, mostly supported by NASA. These have mainly been low voltage circuits using power MOSFET devices.

A 42 V/28 V, 175 W, 50 kHz PWM buck DC-DC converter was designed, fabricated and tested at room temperature and at liquid nitrogen temperature using commercially available components [1-98]. The power circuit was placed in a Dewar flask and the control circuit was at room temperature. The efficiency was found to increase from 95.8 % at room temperature to 97 % at 77 K. The results summarised the overall characteristics at 77 K, but there was no detailed analysis of losses.

The open-loop and closed-loop operation of a 50 kHz, 48±10 V/12 V, 60 W flying capacitor three-level PWM buck converter was reported in [1-99, 1-100] respectively at temperatures down to 77 K using commercially available components. Both the power and control circuits were located in the low temperature environment. The converter was fully functional at 77 K. The voltage variation across the energy transfer capacitors with decreasing temperature resulted in up to 5 V imbalance in the open-loop operation [1-99], which was balanced by the charge-pump controller designed in the close-loop operation [1-100]. However, the conversion efficiency was found to decrease with lower operating temperature, principally due to larger conduction loss in the diodes [1-99, 1-100]. No detailed analysis of power losses in the semiconductors was undertaken. The principal conclusion of the papers was establishing the feasibility of operating a three-level buck converter at low temperatures.

Ref [1-101] explored the operation of a 24 V/48 V, 150 W, 50 kHz boost PWM DC-DC converter over the temperature range of -185°C to 200°C, where the input inductor, the power MOSFET and rectifier were operated at low temperatures, whereas the rest of the power and control circuitry were at room temperature. The room temperature efficiency of 92.2 % decreased to 89.4 % at 200°C, and to 91.5 % at -185°C. On the high temperature side, the efficiency decreased due to increased losses in the power MOSFET, diode, and inductor. However, on the low temperature side, the drop in efficiency was much less because even though the diode and inductor losses increased with decreasing temperatures, the power MOSFET loss decreased due to reductions in the conduction and switching losses [1-101]. The reduction in the MOSFET switching loss was attributed to the decrease in turn-on time and output capacitance at low temperatures [1-101]. However, that conclusion didn't

consider the effect of the improvement in the diode reverse recovery on the MOSFET switching behaviour.

The low temperature performance of a 150 W, 50 kHz, 24 V/48 V boost PWM DC-DC converter was reported in [1-102] at 77 K, using a molypermalloy core-based inductor and a BSCCO-based, high-temperature superconducting inductor. The main objective was to examine the low temperature operation of two types of inductor. The use of the HTS inductor in the converter yielded no significant performance improvement over the same converter with a conventional inductor [1-102]. No description of the semiconductor behaviour at low temperature was given.

1.3.10 Soft-switching converters

As demonstrated by numerous authors, MOSFET conduction losses reduce dramatically with a decrease in temperature; however the temperature dependence of the switching loss is more complicated and depends on the device itself, the driving circuit and the external power circuit. MOSFET switching waveforms were examined experimentally in [1-98] at 300 K and 77 K, an RC snubber was used in each case and it was concluded that the MOSFET switching waveforms were greatly improved with reduced turn-on oscillations. The power MOSFET loss analysis in [1-101] showed that the turn-off loss was almost constant over the temperature range. Several publications have reviewed the use of zero-voltage-switching circuits at low temperatures, the main contributions are summarised in the following paragraphs.

An investigation of hard-switching and soft-switching in a boost converter at 77 K was reported in [1-103] and concluded that the MOSFET turn-on over current transient decreased almost by half in the hard-switching boost converter at 77 K compared with room temperature. Furthermore, the soft-switching circuit consisting of a diode, inductor and capacitor operated successfully at 77 K, and the MOSFET turn-on over current transient decreased further compared with the hard-switching operation at 77 K.

The performance of a 120 W, 100 kHz, 42 V/12 V phase-shifted, zero-voltage-switching, open-loop controlled full-bridge DC-DC converter was reported over the temperature range of -175°C to 25°C in [1-104], using commercially available components. The converter was stable across the temperature range, and a slight increase in efficiency was measured with decreasing temperature, since the decrease in the MOSFET and filter inductor losses were offset by the increase in the diode conduction loss [1-104]. It was pointed out that the use of synchronous rectification in place of diode rectification at the output could further improve the converter efficiency especially at low temperatures due to the decreased conduction loss of MOSFETs [1-104].

Ref [1-105] reported the operation of a 55 W, 200 kHz, 48 V/28 V zero-voltage-switching multi-resonant DC-DC converter at 77 K, using commercially available components. It was found that the values of the resonant inductor and capacitor remained approximately constant with temperature, therefore the switching frequency, resonant frequency and the characteristic impedance did not change significantly, and zero-voltage-switching was maintained [1-105]. There was only a slight increase in efficiency at low temperature since the decrease in the MOSFET on-state loss was offset by the increase in the MOSFET body diode conduction loss [1-105].

A hard-switching boost converter and corresponding soft-switching converters using zero-voltage transition and multi-resonant techniques were examined at liquid nitrogen temperature in [1-106]. Although the zero-voltage-switching converters operated successfully at 77 K, the loss reduction in the main transistors was offset by the increased loss in the resonant components and in the diodes. For this reason the efficiency advantage of the soft-switching converter was lost at low temperatures. It was concluded that the soft-switching converter with a long diode conduction interval had an even lower efficiency in comparison with its hard-switching counterpart [1-106].

1.3.11 High power converters

A chopper circuit made with commercially available MOSFETs and diodes, part of the power conditioning system for a SMES system with a rated energy of 300 J at 130 A, was built and tested in a cryostat at around 80 K to control the superconducting coil current [1-107]. The power loss of the chopper was reduced to half of the value at room temperature and the size of the current leads was greatly reduced. It was concluded that the losses would decrease more by using diodes with lower on-state voltage at low temperature [1-107].

The viability of a 50 kW, MOSFET-based, three-phase inverter at 77 K was demonstrated for utility energy conditioning in [1-108], using a split-capacitor power supply of ± 325 V DC and providing 400 V AC and 72 A RMS line current at 50 kHz. It was shown that the conduction loss could be made extremely small by using parallel MOSFETs, and that the switching loss could be reduced by using soft-switching techniques. Initial results showed that the inverter power loss was approximately 1 % of the rated power. The final aim was to decrease this below 0.5 % at the full 50 kW operation. It was claimed that more work was required to quantify the losses of the various devices in the circuit [1-108].

The patent in [1-109] described the concept of high efficiency cryogenic power conditioning circuit used to convert the DC output of fuel cells into suitable AC power for a vehicle traction drive. The cryogenic cooling was provided by the liquid hydrogen which was then used to supply the fuel cell. It was claimed that the converter at low temperature could exhibit an efficiency of greater than 99 % when driving the motor; furthermore, it was claimed that the reduction in size, weight and cost of the converter could be achieved [1-109]. However, no experimental results were presented.

Ref [1-110] described a patent for a magnetic resonance imaging system. The assumption was that the MOSFET conduction loss could be dramatically reduced by cooling and paralleling while the switching loss could be decreased by using suitable soft-switching

techniques. It was claimed that the system could generate a high magnetic field (1T-2T) for lower cost with higher efficiency, longer lifetime and improved reliability, compared to conventional systems [1-110].

1.3.12 Summary of cryogenic power electronics

According to the foregoing review, most commercial-off-the-shelf power semiconductors and circuits, designed for normal operating temperatures, have the capability of operating at liquid nitrogen temperature, 77 K. Majority carrier devices such as MOSFETs demonstrate improved performance at low temperature, especially lower on-state resistance. Also, the switching losses in minority carrier devices, such as IGBTs and P-i-N diodes, decrease at low temperature due to the decrease in carrier lifetime.

Motivated by the improved power device characteristics at low temperature, the evaluation of power conversion circuits has been performed using different conversion topologies usually at liquid nitrogen temperature, employing power MOSFETs and diodes. However, most published papers have only reported the conversion efficiency at 77 K, and there is little quantitative investigation of power losses for the individual semiconductor devices with temperature. No work was found on the performance of power conversion circuits formed by silicon power semiconductors operating at temperatures below 77 K. Moreover there is very little published work on the comparative performance of different DC-DC converter circuit techniques at cryogenic temperatures, for example soft-switching, synchronous rectifier and multi-level.

1.4 Summary of literature review

The foregoing literature review shows there are an increasing number of superconducting applications in both aerospace and terrestrial fields, creating an impetus for the development of cryogenic power electronics. At the same time, cryogenic semiconductor physics is

maturing, and silicon power semiconductors, such as power diodes, power MOSFETs and IGBTs, are all characterised for low temperature operation. Moreover, power semiconductors made from other materials, such as germanium and silicon germanium, can offer superior switching and on-state performance even at 30 K and appear good options to replace silicon devices in future deep space exploration applications.

Power electronic converters are capable of operating at cryogenic temperatures, in most cases with reduced losses, potentially bringing benefits of increased power density. The potential applications include allowing spacecraft power electronics to operate cold, saving the cost and weight of the environmental control systems. An alternative application is the integration of a power converter into a cryostat with a superconducting device which may increase power density, and depending on the additional energy used by the cryocooler, may also reduce overall system losses. Furthermore, other system benefits may then be possible, for example the use of high voltage, low current feedthroughs into the cryo-system, which would reduce the heat leakage into the system and therefore reduce the load on the cryocooler. To enable such systems to be designed and optimised a better understanding is needed of power converter operation at cryogenic temperatures.

1.5 Scope of the Thesis

From the literature review, the reported work on the cryogenic operation of power conversion circuits is patchy and incomplete; there is insufficient examination of individual semiconductor power losses at low temperatures. The research in this Thesis focuses on the evaluation of semiconductor losses in several MOSFET-based converter circuit technologies across the temperature range 20-300 K.

Chapter 2 examines the semiconductor losses in 500 W, single-transistor, step-down converters operating from 120 V and 500 V DC supplies at temperatures extending down to 20 K. Power MOSFETs and several diode technologies are examined.

Chapter 3 explores the semiconductor losses in two two-transistor, step-down converters at low temperatures. The synchronous rectifier and soft-switching (zero-voltage-switching clamped-voltage) step-down converter are fabricated and evaluated with a 120 V DC supply at temperatures down to 20 K. Also, the synchronous rectifier is evaluated operating with a 500 V DC supply.

Chapter 4 describes the investigation of the semiconductor losses in the three-level, diode-clamped, step-down converter over the temperature range 20-300 K. The prototype operates at 500 W from a 500 V source and at 600 W from a 600 V DC supply. A zero-voltage-switching version of the circuit is proposed to improve the low temperature performance.

Chapter 5 draws conclusions and identifies some of the priorities for further research on cryogenic power electronics.

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Chapter 2

Cryogenic operation of single-transistor step-down converters

This Chapter describes the analysis and experimental measurement of the semiconductor losses in single-transistor step-down converters. Prototypes are examined that operate from 120 V and 500 V supplies, and MOSFET switching devices are employed in each prototype along with several diodes including ultrafast, Schottky and silicon carbide types. The performance of the prototypes is examined at temperatures down to 20 K.

2.1 Step-down converter operation and design

The single-transistor step-down converter, shown in Figure 2-1, consists of a high-frequency switching transistor S_1 which operates with duty ratio D , freewheeling diode D_1 and output filter $L - C_o$. Assuming lossless operation, the output voltage V_o is given by DV_{in} [2-1], where V_{in} is the DC source voltage. C_{in} is a decoupling capacitor which provides the high-frequency AC component of the converter input current. The source current I_{in} is then assumed to be purely DC.

Figure 2-2 displays the main waveforms of the step-down converter in the continuous conduction mode. v_F is the freewheel diode voltage, v_L is the inductor voltage, i_L is the

inductor current with a DC component I_O and a peak-to-peak ripple ΔI_L , v_O is the output capacitor voltage with a DC component V_O and a peak-to-peak ripple ΔV_O , i_{s1} is the transistor current, i_C is the input capacitor current and v_{in} is the input capacitor voltage, which has a DC component V_{in} and a peak-to-peak ripple ΔV_{in} . The difference between the

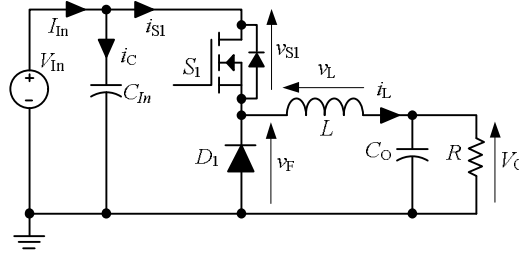


Figure 2-1 Step-down (buck) converter

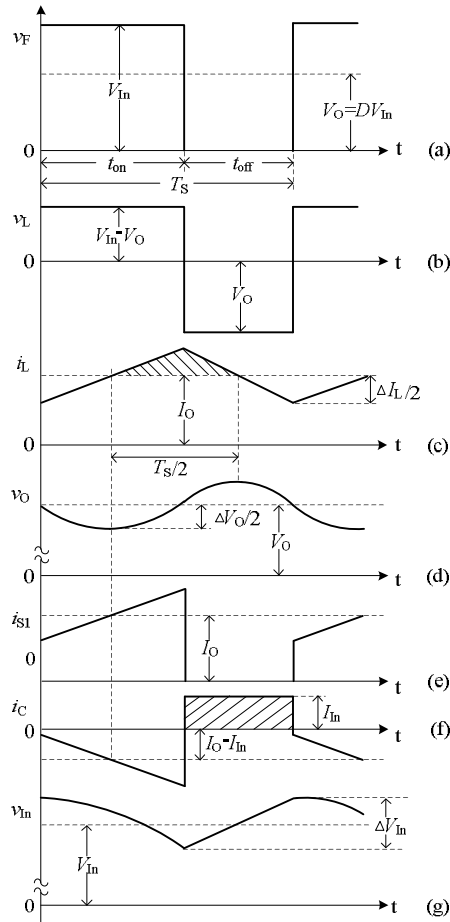


Figure 2-2 Idealised voltage and current waveforms in a buck converter

DC source voltage V_{in} and the capacitor voltage v_{in} is assumed to be dropped across the inductive impedance of the supply cables, which is not shown explicitly.

Based on the analysis of the waveforms and again assuming lossless operation, the design equations for the input capacitor, the filter inductor and the output capacitor are summarised as below.

$$L = \frac{V_o}{\Delta I_L} (1 - D) T_s \quad (2-1)$$

$$C_o = \frac{1}{8L\Delta V_o} V_o (1 - D) T_s^2 \quad (2-2)$$

$$C_{in} = \frac{I_{in} (1 - D) T_s}{\Delta V_{in}} \quad (2-3)$$

where T_s is the switching period.

Table 2-1 Single-transistor converter design requirements

Design Parameters	Converter input voltage V_{in}	
	120 V	500 V
Input current (A)	4	1
Input power (W)	480	500
Output voltage (V)	60	250
Output current (A)	8	2
Duty ratio	50%	50%
Frequency (kHz)	50	50
Input voltage ripple (V)	6	25
Output voltage ripple (V)	0.6	2.5
Inductor current ripple (A)	1.2	0.3

Prototype converters were designed for operation from 120 V and 500 V DC supplies according to the requirements listed in Table 2-1. Applying the requirements to the design

equations resulted in the passive component values for the 120 V and 500 V buck converters, as displayed in Table 2-2. For the 120 V buck converter, the MOSFET IRFB31N20D was selected, and the MOSFET SPP20N60C3 was chosen for the 500 V converter. A Schottky barrier diode, an ultrafast diode and a silicon carbide Schottky barrier diode were selected as freewheel diodes. The breakdown voltage V_{BR} and on-state resistance $R_{DS(on)}$ for the MOSFETs are listed in Table 2-3, and the breakdown voltage and the voltage drop V_F at the rated current for the diodes are listed in Table 2-4. Totally there are three 120 V converters, formed by the low voltage MOSFET and any one of the three diodes, and two 500 V converters, formed by the high voltage MOSFET and either of the two high voltage diodes.

Table 2-2 Passive component design values

Circuit	C_{In}	L	C_o
120 V	6.67 μ F	0.5 mH	5 μ F
500 V	0.4 μ F	8.3 mH	0.3 μ F

Table 2-3 Power MOSFET parameters at 25°C

MOSFETs	V_{BR} (V)	$R_{DS(on)}$ (Ω)
IRFB31N20D	200	0.082
SPP20N60C3	600	0.19

Table 2-4 Power diode parameters at 25°C

Rectifiers	Type	V_{BR} (V)	V_F (V)
MBR20200CT	Silicon Schottky barrier	200	0.85 @10 A
MUR1560	Silicon ultrafast rectifier	600	1.50 @15 A
CSD10060	Silicon carbide Schottky barrier	600	1.80 @10 A

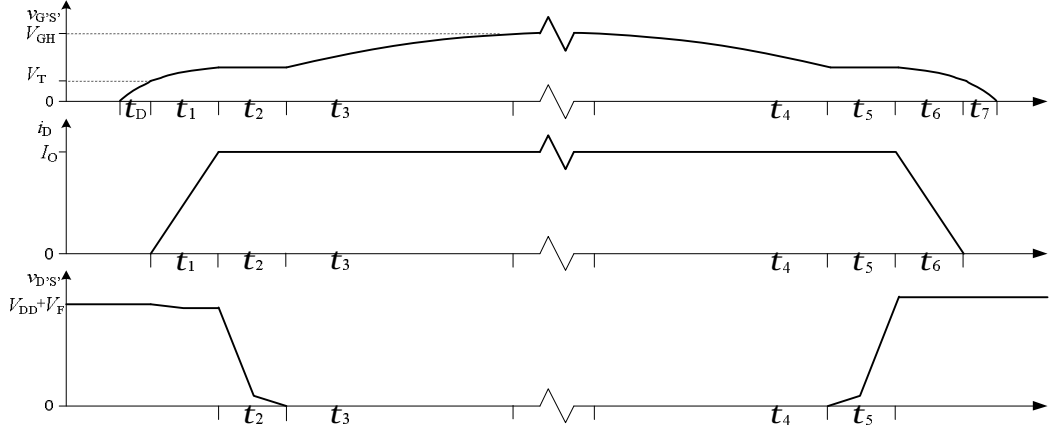


Figure 2-4 MOSFET turn-on and turn-off waveforms

Each switching transition is divided into a sequence of consecutive intervals, plotted in Figure 2-4. The sketched waveforms in Figure 2-4 show the gate-source voltage $v_{G'S'}$, the drain current i_D and the drain-source voltage $v_{D'S'}$.

2.2.1.1 MOSFET turn-on analysis

Initially the MOSFET is assumed to be turned off and the load current I_O circulates through the freewheel diode. The gate-source voltage $v_{G'S'}$ is below the threshold voltage V_T , the drain current i_D is zero and the drain-source voltage $v_{D'S'}$ equals v_{DS} which has a value of $V_{DD} + V_F$, V_F is the forward voltage drop of freewheel diode in Figure 2-3. The gate drive voltage v_{GG} then switches instantaneously to the high level of V_{GH} from zero. The subsequent turn-on transient is typically divided into four parts as shown in Figure 2-4.

The first part is the delay time t_D , during which capacitors $C_{G'S'}$ and $C_{G'D'}$ are charged via gate resistance $R_G + R_{G'}$ and the gate voltage increases exponentially until $v_{G'S'} = V_T$ according to (2-4), whilst $i_D = 0$ and $v_{D'S'} = v_{DS} = V_{DD} + V_F$.

$$v_{G'S'} = V_{GH} [1 - \exp(-t/t_G)] \quad (2-4)$$

where

$$t_G = (R_G + R_{G'})(C_{G'S'} + C_{G'D'}) \quad (2-5)$$

An expression for t_D may be obtained by setting $v_{G'S'} = V_T$ and $t = t_D$ in (2-4).

$$t_D = t_G \ln\left(\frac{V_{GH}}{V_{GH} - V_T}\right) \quad (2-6)$$

Once the gate-source voltage is above the threshold voltage, $v_{G'S'} > V_T$, the MOSFET enters the second stage of the transient, denoted t_1 in Figure 2-4, during which both drain current and drain-source voltage are non-zero, generating switching loss. In order to obtain analytical solutions for t_1 , the source lead inductance L_S is neglected. The simplified equivalent circuit is redrawn in Figure 2-5.

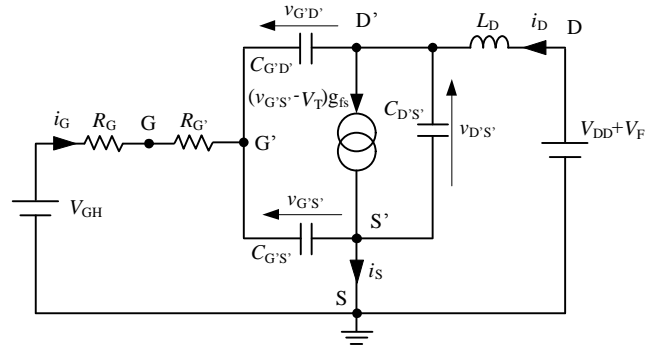


Figure 2-5 Simplified equivalent circuit during t_1

During t_1 the drain current increases from zero to I_O , the current level in the inductive load, at which point the freewheel diode becomes reverse biased. The gate-source voltage rises from V_T to the plateau value $V_T + I_O / g_{fs}$, and the drain-source voltage drops slightly from

$V_{DD} + V_F$ due to the increasing drain current in the parasitic inductance. The gate current is the sum of the $C_{G'S'}$ and $C_{G'D'}$ charging currents in (2-7).

$$i_G = C_{G'S'} \frac{dv_{G'S'}}{dt} + C_{G'D'} \frac{dv_{G'D'}}{dt} = \frac{V_{GH} - v_{G'S'}}{R_G + R_{G'}} \quad (2-7)$$

The drain current is expressed in (2-8).

$$\frac{di_D}{dt} = \frac{V_{DD} + V_F - v_{D'S'}}{L_D} \quad (2-8)$$

$$i_D = \int \frac{V_{DD} + V_F - v_{D'S'}}{L_D} dt \quad (2-9)$$

Summing the currents at node S' , Figure 2-5, the source current can be expressed by (2-10), where the channel current equals $g_{fs}(v_{G'S'} - V_T)$ according to the MOSFET characteristic.

$$i_S = g_{fs}(v_{G'S'} - V_T) + C_{G'S'} \frac{dv_{G'S'}}{dt} + C_{D'S'} \frac{dv_{D'S'}}{dt} \quad (2-10)$$

Using Kirchhoff's current law, the source current is the total of the gate and drain currents.

$$i_S = i_G + i_D \quad (2-11)$$

Substituting (2-7), (2-9) and (2-10) into (2-11) and re-arranging, the drain-source voltage is expressed in (2-12)

$$L_D C_{D'S'} \frac{d^2 v_{D'S'}}{dt^2} + v_{D'S'} = V_{DD} + V_F - L_D \left[(g_{fs} + \frac{1}{R_G + R_{G'}}) \frac{dv_{G'S'}}{dt} + C_{G'S'} \frac{d^2 v_{G'S'}}{dt^2} \right] \quad (2-12)$$

The gate-drain voltage is obtained in (2-13) by rearranging (2-7)

$$C_{G'D'} \frac{dv_{G'D'}}{dt} = \frac{V_{GH} - v_{G'S'}}{R_G + R_{G'}} - C_{G'S'} \frac{dv_{G'S'}}{dt} \quad (2-13)$$

Applying Laplace transforms to (2-12) and (2-13), denoting the Laplace operator by s and neglecting the initial voltages across the capacitors since the product of the voltage and capacitance is relatively small [2-2, 2-3],

$$v_{D'S'}(s) = \frac{V_{DD} + V_F - sL_D[g_{fs} + 1/(R_G + R_{G'}) + sC_{G'S'}]v_{G'S'}(s)}{1 + s^2L_D C_{D'S'}} \quad (2-14)$$

$$v_{G'D'}(s) = \frac{(V_{GH} - v_{G'S'}(s))/(R_G + R_{G'}) - sC_{G'S'}v_{G'S'}(s)}{sC_{G'D'}} \quad (2-15)$$

Using Kirchhoff's voltage law, the gate-source voltage is the sum of $v_{G'D'}$ and $v_{D'S'}$ in (2-16).

$$v_{G'S'}(s) = v_{G'D'}(s) + v_{D'S'}(s) \quad (2-16)$$

Substituting (2-14) and (2-15) into (2-16) and rearranging, the gate-source voltage is expressed in (2-17). The detailed calculation is seen in Appendix 1.

$$v_{G'S'}(s) = \frac{V_{GH}}{s^3 t_{G3}^3 + s^2 t_{G2}^2 + s t_G + 1} \quad (2-17)$$

where

$$t_{G3}^3 = L_D(R_G + R_{G'})(C_{G'D'}C_{G'S'} + C_{G'S'}C_{D'S'} + C_{D'S'}C_{G'D'})$$

$$t_{G2}^2 = L_D\{C_{D'S'} + C_{G'D'}[1 + g_{fs}(R_G + R_{G'})]\}$$

t_G is given by (2-5). Given that the product of either two inter-electrode capacitances is orders of magnitude less than the single capacitance [2-1, 2-2], t_{G3}^3 is neglected. Assuming $g_{fs}(R_G + R_{G'}) \gg 1$, which is usually the case for power MOSFETs with high drain current ratings [2-1, 2-2], (2-17) reduces to

$$v_{G'S'}(s) = \frac{V_{GH}}{s^2 t_m t_{G'} + s t_G + 1} \quad (2-18)$$

where $t_m = g_{fs}L_D$ and $t_{G'} = C_{G'D'}(R_G + R_{G'})$.

The equation (2-18) may be solved to either sinusoidal or exponential solutions [2-3]. Since t_G^2 is greater than $4t_m t_{G'}$ in the converters considered in this Thesis, an exponential solution

is given in (2-19) for $v_{G'S'}$ [2-4], assuming the initial conditions are $v_{G'S'} = V_T$ and $di_D / dt = 0$.

$$v_{G'S'} = V_{GH} - (V_{GH} - V_T) \frac{t_b \exp(-t/t_b) - t_c \exp(-t/t_c)}{t_b - t_c} \quad (2-19)$$

Provided that $v_{GS} > V_T$ and $v_{DS} > i_D R_{DS(on)}$ during t_1 [2-2], the drain current is calculated by $i_D = g_{fs}(v_{G'S'} - V_T)$. Substituting for $v_{G'S'}$ from (2-19) results in (2-20).

$$i_D = g_{fs}(V_{GH} - V_T) \left(1 - \frac{t_b \exp(-t/t_b) - t_c \exp(-t/t_c)}{t_b - t_c}\right) \quad (2-20)$$

t_1 is obtained by setting i_D equal to I_O in (2-20) and solving for t .

Differentiating (2-20) to obtain an expression for di_D / dt , then substituting into (2-8) results in the expression for $v_{D'S'}$.

$$v_{D'S'} = V_{DD} + V_F - g_{fs} L_D (V_{GH} - V_T) \frac{\exp(-t/t_b) - \exp(-t/t_c)}{t_b - t_c} \quad (2-21)$$

where

$$t_b = \frac{2t_m t_{G'}}{t_G - (t_G^2 - 4t_m t_{G'})^{1/2}} \quad (2-22)$$

$$t_c = \frac{2t_m t_{G'}}{t_G + (t_G^2 - 4t_m t_{G'})^{1/2}} \quad (2-23)$$

During the third stage of the transient, denoted t_2 in Figure 2-4, the drain-source voltage decreases from V_{D*} , the value at the end of t_1 , to zero, whilst $C_{G'D'}$ is charged by the gate current. In this period both i_D and $v_{G'S'}$ remain constant with values of I_O and $V_T + I_O / g_{fs}$ respectively. The equivalent circuit is displayed in Figure 2-6. The analysis neglects diode reverse recovery, resulting in the waveforms shown in Figure 2-4.

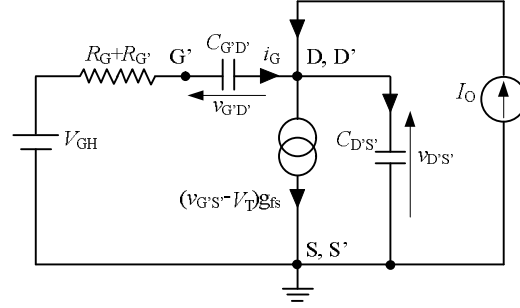


Figure 2-6 Equivalent circuit for the fall of the drain voltage

Summing currents at the node D' in Figure 2-6 gives

$$g_{fs}(v_{G'S'} - V_T) + C_{D'S'} \frac{dv_{D'S'}}{dt} = I_O + C_{G'D'} \frac{dv_{G'D'}}{dt} \quad (2-24)$$

and the gate-source voltage is expressed in (2-25) from Figure 2-6.

$$v_{G'S'} = V_{GH} - (R_G + R_{G'}) C_{G'D'} \frac{dv_{G'D'}}{dt} \quad (2-25)$$

Since $v_{G'S'}$ is constant, $dv_{G'D'}/dt = -dv_{D'S'}/dt$. Rearranging (2-24) and substituting (2-25) for $v_{G'S'}$ results in

$$\frac{dv_{D'S'}}{dt} = \frac{I_O - g_{fs}(V_{GH} - V_T)}{C_{D'S'} + [1 + g_{fs}(R_G + R_{G'})]C_{G'D'}} \quad (2-26)$$

The right hand side of (2-26) is a constant and its magnitude is denoted K , therefore

$$v_{D'S'} = V_{D^*} - Kt \quad (2-27)$$

Practically $C_{G'D'}$ increases as $v_{D'S'}$ decreases. The change in $C_{G'D'}$ with $v_{D'S'}$, Figure 2-7, reduces the value of K sharply at the end of this period, slowing the fall in $v_{D'S'}$. For

approximate calculations of switching waveforms, the capacitance is assumed to take the discrete values $C_{G'D'}$ and $C_{G'D''}$ in Figure 2-7 the transition occurring at $v_{D'S'} = v_{G'S'}$ [2-1].

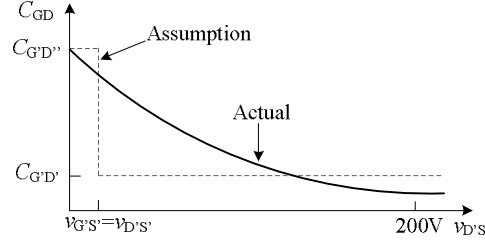


Figure 2-7 Variation in gate-drain capacitance with drain-source voltage [2-1]

Accordingly, t_2 is separated into two parts in Figure 2-4. During the first part of t_2 , $v_{D'S'}$ is assumed to fall rapidly to $v_{G'S'}$, which equals $V_T + I_O / g_{fs}$, while in the second part of t_2 , $v_{D'S'}$ declines much more slowly due to the increased capacitance value. The two values of K in (2-27) are denoted K_1 and K_2 .

$$K_1 = \frac{g_{fs}(V_{GH} - V_T) - I_O}{C_{D'S'} + [(1 + g_{fs}(R_G + R_{G'}))C_{G'D'}]} \quad (2-28)$$

$$K_2 = \frac{g_{fs}(V_{GH} - V_T) - I_O}{C_{D'S'} + [(1 + g_{fs}(R_G + R_{G'}))C_{G'D''}]} \quad (2-29)$$

The duration of t_2 is determined by (2-30)

$$t_2 = \frac{V_{D^*} - (V_T + I_O / g_{fs})}{K_1} + \frac{V_T + I_O / g_{fs}}{K_2} \quad (2-30)$$

At the end of t_2 the MOSFET completes the main switching transition and is in the forward conducting state. During the final stage of the turn-on transient, denoted t_3 in Figure 2-4, the MOSFET input capacitances are charged via $R_G + R_{G'}$ to the gate drive voltage V_{GH} .

2.2.1.2 MOSFET turn-off analysis

Figure 2-4 also plots the four stages of the MOSFET turn-off transient. The MOSFET equivalent circuit of Figure 2-3 still applies, but now the initial conditions are that $v_{D'S'}$ is almost zero and the load current I_O flows through the conducting MOSFET with $v_{G'S'} = V_{GH}$. At the turn-off instant the gate supply voltage V_{GG} drops instantaneously to zero. The gate voltage begins to fall, discharging $C_{G'S'}$ and $C_{G'D'}$. As long as $v_{G'S'} > V_T + I_O / g_{fs}$, I_O continues to flow through the MOSFET and $v_{D'S'}$ is unaffected. The time taken for $v_{G'S'}$ to fall to $V_T + I_O / g_{fs}$ is the turn-off delay time denoted t_4 in Figure 2-4.

During the next stage of turn-off, denoted t_5 in Figure 2-4, $v_{D'S'}$ starts rising whilst the full load current continues to flow in the MOSFET. i_D stays constant at the value I_O and $v_{G'S'}$ remains constant at the value $V_T + I_O / g_{fs}$. The equivalent circuit is the same as that in Figure 2-6, and the analysis is similar, but with different initial conditions. The drain-source voltage $v_{D'S'}$ rises to $V_{DD} + V_F$ according to $v_{D'S'} = Kt$, where, to account for the non-linear gate-drain capacitor, K takes the values:

$$K = K_3 = \frac{I_O + g_{fs} V_T}{C_{D'S'} + [(1 + g_{fs} (R_G + R_{G'})) C_{G'D'}]} \text{ for } v_{D'S'} < V_T + I_O / g_{fs} \quad (2-31)$$

$$K = K_4 = \frac{I_O + g_{fs} V_T}{C_{D'S'} + [(1 + g_{fs} (R_G + R_{G'})) C_{G'D'}]} \text{ for } v_{D'S'} \geq V_T + I_O / g_{fs} \quad (2-32)$$

The duration of t_5 is determined by (2-33)

$$t_5 = \frac{V_T + I_O / g_{fs}}{K_3} + \frac{V_{DD} + V_F - (V_T + I_O / g_{fs})}{K_4} \quad (2-33)$$

When $v_{D'S'}$ reaches $V_{DD} + V_F$, the diode becomes forward biased and the turn-off transient enters the third stage, denoted t_6 in Figure 2-4. i_D starts to fall from I_O to zero whilst $v_{D'S'}$ rises as the circuit dictates. The equivalent circuit is then that of Figure 2-5, and the analysis is similar to that in the turn-on stage t_1 with new conditions, $V_{GH} = 0$ and $v_{G'S'}$ drops from $V_T + I_O / g_{fs}$ to V_T . The exponential solutions are as follows,

$$v_{G'S'} = (V_T + I_O / g_{fs}) \frac{t_b \exp(-t/t_b) - t_c \exp(-t/t_c)}{t_b - t_c} \quad (2-34)$$

$$i_D = (g_{fs} V_T + I_O) \frac{t_b \exp(-t/t_b) - t_c \exp(-t/t_c)}{t_b - t_c} - g_{fs} V_T \quad (2-35)$$

$$v_{D'S'} = V_{DD} + V_F + L_D (g_{fs} V_T + I_O) \frac{\exp(-t/t_b) - \exp(-t/t_c)}{t_b - t_c} \quad (2-36)$$

t_6 is obtained by setting i_D equal to zero in (2-35) and solving for t .

In the last stage, t_7 in Figure 2-4, the MOSFET is non-conducting and the gate capacitance continues discharging via $R_G + R_{G'}$. $v_{G'S'}$ exponentially approaches zero with a time constant t_G determined by (2-5), this final stage corresponds to the delay time in the turn-on transient.

2.2.1.3 MOSFET turn-on considering diode reverse recovery

The foregoing MOSFET turn-on analysis is based on the assumption that the freewheeling diode D_1 is ideal in Figure 2-3. However, in practice the MOSFET turn-on waveforms will be modified by the reverse recovery of the freewheel diode. The transistor turn-on waveforms are plotted in Figure 2-8 considering the diode reverse recovery.

When the MOSFET is in the off state and the diode conducts the current I_O , and minority carriers are stored in the diode. When the MOSFET turns on, negative current flows through the diode, which actively sweeps out the minority carriers stored in the junction. The current

rate of change is typically limited by the turn-on of the MOSFET, the package inductance and other stray inductances present in the external circuit; therefore the peak magnitude of the reverse current I_{RR} depends on the external circuit, and can be many times larger than the forward current I_O , Figure 2-8 (b).

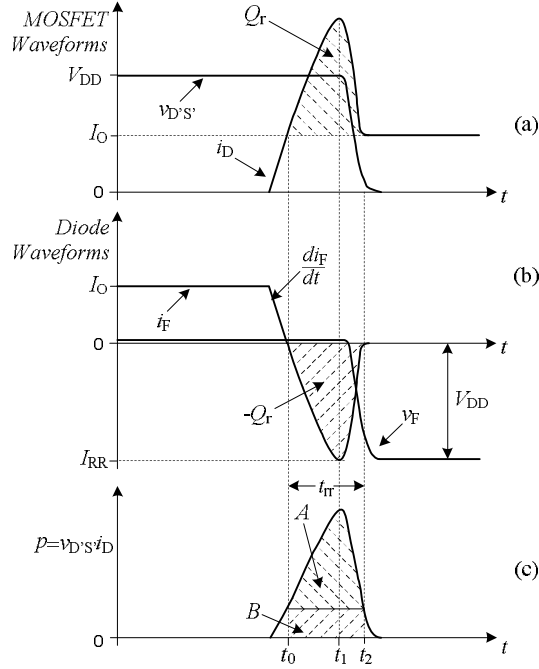


Figure 2-8 Transistor turn-on waveforms considering diode reverse recovery [2-4]

The reverse recovery charge Q_r is defined as the time integral of the reverse current during the reverse recovery period t_{rr} , the interval of $(t_2 - t_0)$ in Figure 2-8 [2-5].

$$Q_r = \int_{t_0}^{t_2} |i_F| dt \quad (2-37)$$

Approximating the waveform by straight lines, Q_r can be expressed as

$$Q_r = \frac{1}{2} I_{RR} (t_2 - t_0) = \frac{1}{2} (t_1 - t_0) \frac{di_F}{dt} (t_2 - t_0) \quad (2-38)$$

where di_F / dt is the rate of fall of the diode current.

Diodes in which the interval $(t_2 - t_1)$ is short compared to $(t_1 - t_0)$, Figure 2-8, are called abrupt-recovery diodes, and so $t_1 - t_0 \approx t_{rr}$. Equation (2-38) may be simplified into (2-39) for the Q_r calculation in abrupt-recovery diodes [2-5, 2-6].

$$Q_r = \frac{1}{2} \frac{di_F}{dt} t_{rr}^2 \quad (2-39)$$

Diode reverse recovery affects the MOSFET switching waveforms as indicated in Figure 2-8 (a). The MOSFET drain current must now rise to the load current level plus the peak diode reverse recovery current before the diode can block reverse voltage and allow $v_{D'S'}$ to fall. As a result the MOSFET turn-on loss increases. The instantaneous power dissipated in the MOSFET is also sketched in Figure 2-8 (c), and the additional energy lost is (2-40).

$$W_{MOSFET} = \int_{t_0}^{t_2} v_{D'S'} i_D dt \quad (2-40)$$

For an abrupt-recovery diode, the integral can be evaluated simply, $v_{D'S'}$ is then equal to V_{DD} for essentially the entire diode recovery interval $t_{rr} \approx t_1 - t_0$, and $i_D = I_O - i_F$.

$$W_{MOSFET} = \int_{t_0}^{t_1} V_{DD} (I_O - i_F) dt = V_{DD} I_O t_{rr} + V_{DD} Q_r \quad (2-41)$$

where $V_{DD} Q_r$ and $V_{DD} I_O t_{rr}$ correspond to the areas A and B , Figure 2-8 (c). The diode recovery leads directly to the average additional power loss $W_{MOSFET} f_s$, where f_s is the switching frequency.

2.2.2 Switching loss validation at room temperature

The single-transistor step-down converter employs power MOSFET IRFB31N20D to switch 8 A (I_O) with 120 V (V_{DD}) at 50 kHz, and two gate resistors with 20 Ω and 5.6 Ω were used to control the drain current rising and decreasing times respectively with $V_{GH} = 12V$. The

MOSFET parameters related to the switching loss calculation are listed in Table 2-5, which were obtained from the IRFB31N20D datasheet. Values of the MOSFET lead inductances are typically in the region of 5-15 nH [2-2], so $L_D = 10\text{nH}$.

Table 2-5 IRFB31N20D parameters at 25°C

Parameter	Units	Typ.
g_{fs}	S	17
L_D	nH	10
V_T	V	4
$C_{G'S'}$	pF	2292
$C_{G'D'}$	pF	50
$C_{G'D''}$	pF	1000
$C_{D'S'}$	pF	170

The MOSFET drain-source voltage and drain current during the individual switching intervals were calculated using the foregoing analytical equations (2-20), (2-21), (2-26) to (2-33), (2-35) and (2-36). The circuit stray inductance, which was principally attributed to the planar bus bar connecting the MOSFET and diode to the input capacitor C_m , was estimated to be 70 nH by the inductance calculation for parallel conducting sheets in [2-7]. So L_D was increased to 80 nH. Also the diode output capacitance of 100 pF was included by increasing the MOSFET output capacitance to 270 pF. The durations of principal switching intervals were obtained using the equations (2-20), (2-30), (2-33) and (2-35), and are listed in Table 2-6 for the MOSFET turn-on and turn-off transitions.

The 120 V buck converters were tested at room temperature with three different power diodes, ultrafast, Schottky and silicon carbide Schottky diodes. The measured switching times are listed in Table 2-6 from the experimental waveforms, denoted by Ult, Sch and SiC respectively. The discrepancies in the predicted and measured values of t_2 were attributed to the diode reverse recovery process. Otherwise the predictions show good agreement with the measurements considering the approximations made in the analysis.

Table 2-6 Calculated and measured MOSFET turn-on and turn-off times

Items	Units	Calculated	Measured values		
			Ult	Sch	SiC
τ_1	ns	25	28	27	29
τ_2	ns	30	47	31	26
τ_5	ns	14	15	16	19
τ_6	ns	23	17	18	21
di/dt (rising)	A/ns	0.32	0.29	0.30	0.28
di/dt (falling)	A/ns	0.35	0.47	0.44	0.38

Table 2-7 Calculated and measured MOSFET turn-on and turn-off losses

Switching loss	Units	Calculated	Measured values		
			Ult	Sch	SiC
MOSFET turn-on	W	0.70	3.22	2.00	1.03
MOSFET turn-off	W	0.95	0.57	0.54	0.51

The switching losses were calculated by time integration of the device current and voltage product multiplied by the switching frequency, Table 2-7, using the calculated and measured switching waveforms, Figure 2-9. Examination of Figure 2-9 shows that there is a large pulse of forward current through the MOSFET at turn-on in the prototype with the ultrafast diode due to the diode reverse recovery, which was thought to account for the large difference in the predicted and measured MOSFET turn-on losses. Using the equations (2-39) and (2-41), di/dt (50 A/ μ s) and reverse recovery time (60 ns) from the ultrafast diode data sheet, the additional MOSFET turn-on loss was calculated to be 3.4 W. The di/dt in the practical waveforms is however over six times this figure.

The difference in the MOSFET turn-off losses between the predicted and measured values may be caused by the piecewise linear approximation for the MOSFET non-linear gate-drain capacitance. Moreover, in practice both drain-source capacitor and transconductance are dependent on the drain-source voltage, which, however, are constant in the analytical

calculations. The turn-off oscillations at about 29 MHz in the measured waveforms were attributed to the stray inductance ringing with device capacitance. The natural frequency of the stray inductance (80 nH) and the device capacitance (270 pF) is 34.2 MHz.

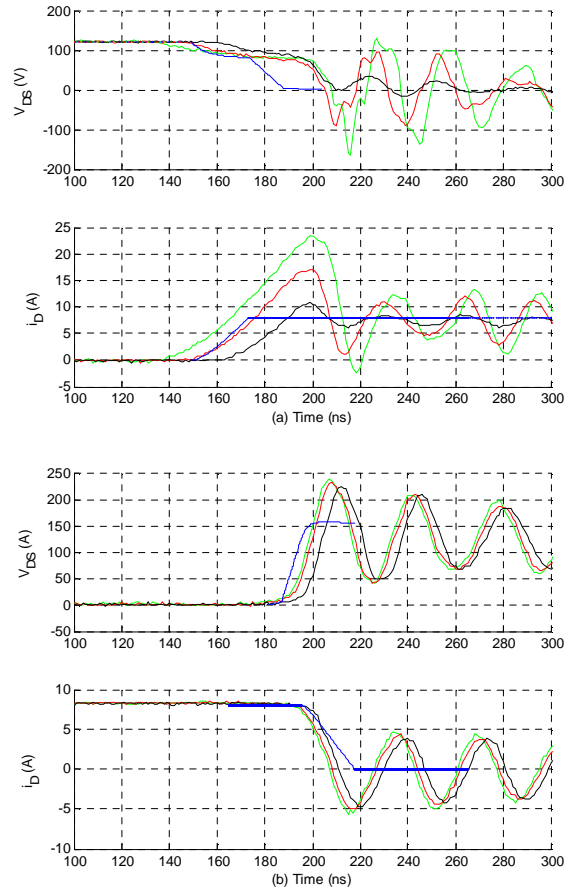


Figure 2-9 Predicated and measured MOSFET switching waveforms: (a) turn-on, (b) turn-off; blue: analytical result; green: with ultrafast diode; red: with Schottky diode; black: with SiC diode

2.3 Cryogenic system introduction

The cryogenic system is built around a COOLPOWER 120 T cold head from Leybold Vacuum GmbH which is powered by a sealed liquid helium cooling circuit. The temperature of the cold head can be decreased to 20 K in approximately 50 minutes, and the refrigeration unit has a cooling capacity of 120 W at 80 K providing the capability to operate power conversion circuits and power devices continuously at low temperatures.

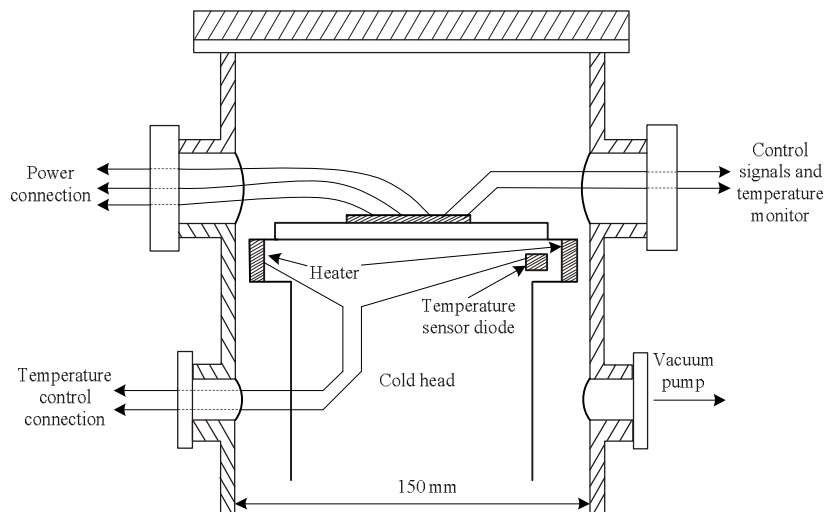


Figure 2-10 Cold chamber cross section

Figure 2-10 shows the cross section of the cold chamber. The test sample is mounted on the cold head inside the chamber. The cold head diameter is 120 mm. A vacuum jacket surrounds the cold head to prevent convection heating of the devices and water condensation. The vacuum is provided by a two-stage pumping system, a turbo molecular pump Turbotronik NT10 backed by a rotary vane pump Trivac D4B. The vacuum level is monitored by a vacuum gauge ITR 90. During the cryogenic tests, the pressure inside the cold chamber is below 10^{-6} bar. Under that vacuum level voltages in the region of 600 V can be safely used in the chamber. A dry nitrogen supply is used to release the vacuum after the experimental work to avoid condensation of water vapour.

The cold chamber has two feedthroughs for connection with the sample. One feedthrough is employed for high power connections, on the left hand side in Figure 2-10, and a 12-pin instrumentation feedthrough on the right hand side is used for signal connections, where 8 pins are used for control signals and measurement and 4 pins for the temperature monitor. The temperature sensing diode has an accuracy of ± 1 K for temperatures below 100 K and may be mounted directly next to or on top of a particular component in the test circuit.

A second temperature sensing diode is embedded within the cold head along with a 160 W heater coil, Figure 2-10. Together with an external power supply and control loop shown in Appendix 2, the diode and heater coil provide a mechanism for regulating the cold head temperature within the range 20-120 K. Photographs of the overall experimental system are shown in Appendix 3.

2.4 Power semiconductor characteristics at low temperatures

The on-state and breakdown voltage characteristics of the MOSFETs and diodes were measured using high precision multi-meters. In the case of the on-state measurement, an 8 A current pulse was used for the low voltage components and a 2 A pulse for the high voltage devices. The duration of the current pulse was about one second. The MOSFET gate-source voltage was set at 12 V during the on-state tests. The breakdown voltage characteristics were measured with a 1 M Ω resistor connected in series with the device, and the MOSFET gate and source were shorted together. The breakdown voltage was taken to be the voltage at which the leakage current was 100 μ A. The threshold voltages of the IRFB31N20D were also measured at the drain currents of 0.25 mA, 0.5 mA, 1.0 mA and 10 mA using high precision multi-meters, and the device transconductance was estimated by using curve fitting techniques to obtain the gradient of the linear part of the i_D, v_{GS} curves measured by a digital oscilloscope. The test circuits are displayed in Appendix 4.

2.4.1 Power MOSFET characteristics at low temperatures

The on-state resistances of the IRFB31N20D and SPP20N60C3 MOSFETs are plotted in Figure 2-11 over the temperature range 20-300 K. The error between the measured device case temperature and the junction temperature was estimated using the data sheet thermal resistance to be 3 °C at room temperature. At low temperatures the junction-to-case temperature difference becomes lower due to the decreased thermal resistance of the material, the thermal conductivity of silicon and many substrates increases by a factor 5-10 at 77 K [2-8].

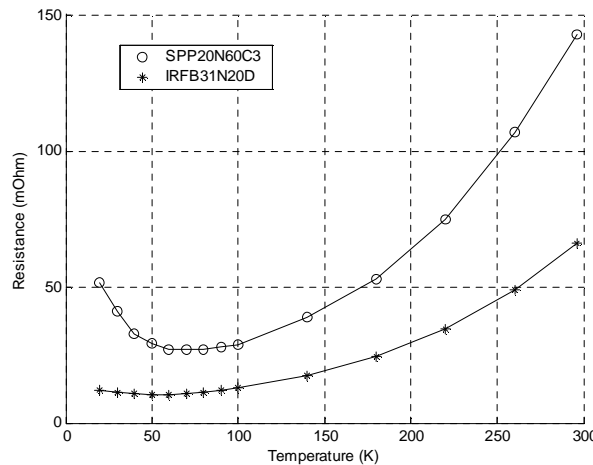


Figure 2-11 Measured MOSFET on-state resistances, $V_{GS} = 12V$
 $I_D = 8A$ for the IRFB31N20D and $I_D = 2A$ for the SPP20N60C3

The IRFB31N20D, Figure 2-11, has a minimum resistance at 50 K of 10.3 mΩ, less than one-sixth of the room temperature value under the forward current of 8 A. The SPP20N60C3 on-state resistance at 2 A current reaches a minimum of 26.8 mΩ at 70 K, less than one-fifth of the room temperature value.

These results appear to be inconsistent with most published work on the subject, where, as described in Section 1.3.3, higher voltage MOSFETs tend to exhibit a larger reduction in $R_{DS(on)}$ at cryogenic temperatures than do low voltage devices. This is due to the greater

temperature sensitivity of the drift region resistance, which is normally the dominant resistance in high voltage devices [2-9].

The smaller than expected reduction in the on-state resistance of the SPP20N60C3 device was attributed to the device's CoolMOS structure, Figure 2-12, whereby compensation p -stripes are inserted in the vertical drift region. The doping of the drift region is then increased by an order of magnitude and the vertical p -stripes compensate the surplus current conducting n -charges [2-10]. Using this technique, the on-state resistance of a 600 V MOSFET can be decreased to one-fifth of that of a conventional device [2-10].

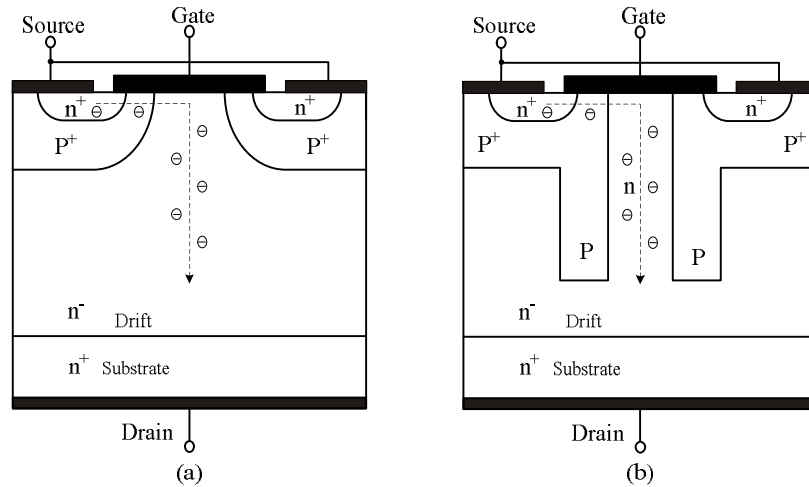


Figure 2-12 Structure of MOSFET: (a) conventional, (b) CoolMOS

The increase in resistance at very low temperature, Figure 2-11, results from reduced carrier availability, referred to as carrier freeze-out. The carrier freeze-out effect is more significant in the JFET and the drift regions which dominate the resistance of MOSFETs with high voltage ratings [2-9].

Figure 2-13 displays the breakdown voltage of the IRFB31N20D and SPP20N60C3 at temperatures down to 20 K from 300 K. As expected, both breakdown voltages decrease with a reduction in temperature. The breakdown voltage of the SPP20N60C3 reduces by

more than 24 % at 20 K compared with room temperature, and the reduction is 23 % for the IRFB31N20D.

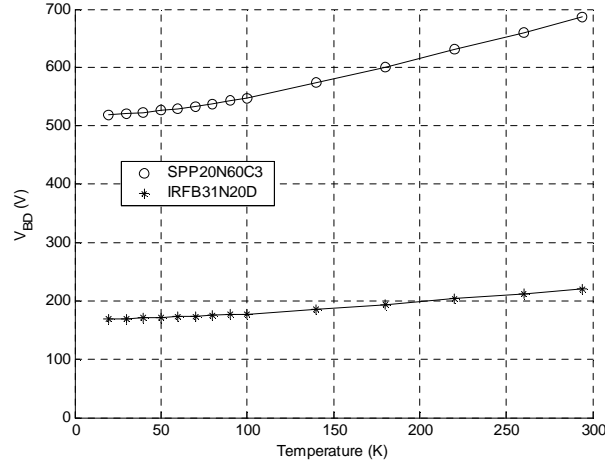


Figure 2-13 Measured MOSFET breakdown voltages

The threshold voltages are plotted in Figure 2-14 for the IRFB31N20D across the temperature range 20-300 K at the drain currents of 0.25 mA, 0.5 mA 1.0 mA and 10 mA. The threshold voltage increases by 24-29 % at 20 K, attributed to the fall in intrinsic carrier concentration at low temperatures resulting in a larger gate-source voltage being needed to form the inversion layer [2-9]. The variation in transconductance is plotted in Figure 2-15, and it increases by 70 % at 20 K due to the increase in inversion layer mobility at low temperatures [2-9]. The increase in threshold voltage is similar to that reported in the literature for other devices, Section 1.3.3; however the increase in transconductance is much lower than that reporting elsewhere, suggesting that the change in transconductance is device dependent.

Using the threshold voltage and transconductance at 20 K and the switching loss calculations in Section 2.2.2, the turn-on loss was calculated and increased from 0.70 W at room temperature, Table 2-7, to 0.96 W, whereas the turn-off loss decreased from 0.95 W at room temperature, Table 2-7, to 0.73 W, not considering the variation in the gate resistance and inter-electrode capacitances at low temperatures. This suggests that the total MOSFET switching losses will not vary significantly at cryogenic temperatures.

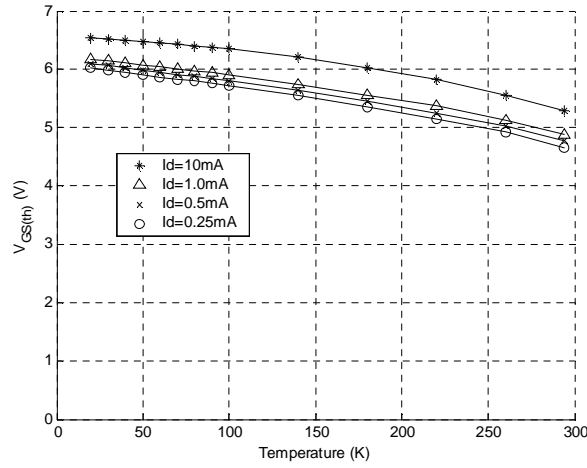


Figure 2-14 Measured threshold voltages for the IRFB31N20D

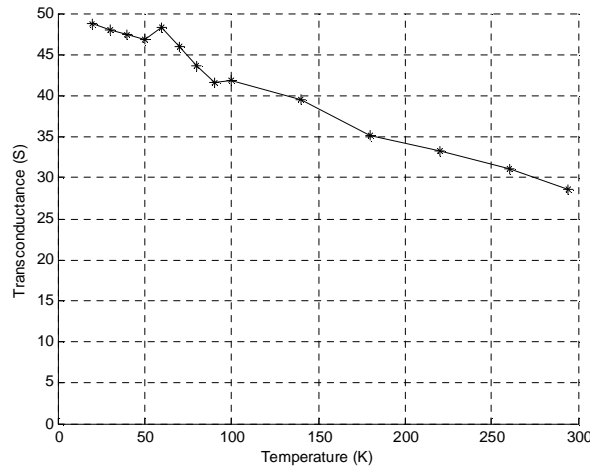


Figure 2-15 Measured transconductance for the IRFB31N20D

Apart from the on-state resistance, the breakdown voltage, the threshold voltage and the transconductance which change significantly with temperature, many of the parameters in the equations presented for the analysis of MOSFET switching behaviour such as the parasitic capacitances and inductances are relatively insensitive to temperature, a small reduction in the values of the parasitic capacitances has been reported in [2-9, 2-11, 2-12] at very low temperatures. Together these effects are likely to result in a small increase in switching speed and a reduction in switching losses; however the extent of the change will vary between devices and circuit applications.

2.4.2 Power diode characteristics at low temperatures

The on-state voltages of the three diodes at 8 A are plotted in Figure 2-16 against case temperature from 300 K to 20 K. At room temperature the temperature difference between junction and case was estimated to be 6-8 °C. This will reduce at low temperature due to the significant decrease in the thermal resistance. Figure 2-16 shows that the silicon carbide diode has the largest voltage drop while the Schottky diode has the lowest. The overall trend seen in each of the three sets of measured data is an increase in voltage at low temperatures. The proportionate increase is greatest for the MBR20200CT, 30 %, and smallest for the MUR1560, 20 %. The slightly different shapes seen in the three sets of data were attributed to the differing contributions made to the total on-state voltages by the blocking drift region which has a positive temperature coefficient and the metal-semiconductor voltage drop in the Schottky devices which has a negative temperature coefficient and the p - n junction voltage drop in the P-i-N diode which also has a negative temperature coefficient. The MUR1560 and CSD10060 on-state voltages at 2 A are plotted in Figure 2-17 where the changed contributions of the two parts of the on-state voltages account for the differences with the 8 A measurements.

Figure 2-18 displays the breakdown voltages of the diodes in the temperature range 20-300K. Both the silicon Schottky and the ultrafast diodes have positive temperature coefficients in their breakdown voltages; however there is a negative temperature coefficient in the breakdown voltage of the silicon carbide diode. At low temperatures the leakage current in SiC diodes is dominated by band-to-band tunnelling [2-13], not impact ionisation as in p - n junctions [2-14]. The breakdown voltage due to the tunnelling effect has a negative temperature coefficient [2-15]. Therefore, the SiC diode breakdown voltage rises with decreasing temperature. However, the second generation silicon carbide diodes have a breakdown voltage with a positive temperature coefficient [2-16].

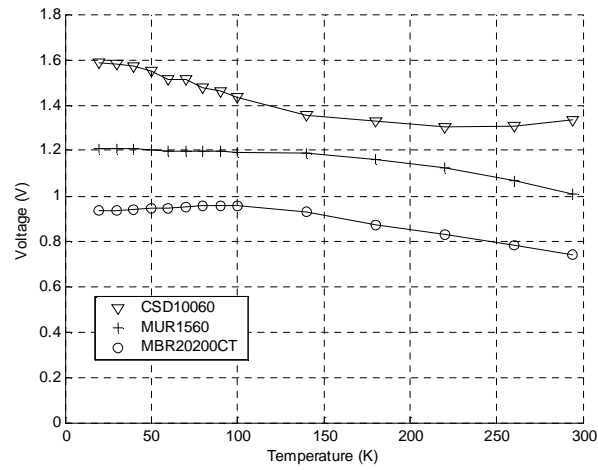


Figure 2-16 Measured diode on-state voltages at 8 A

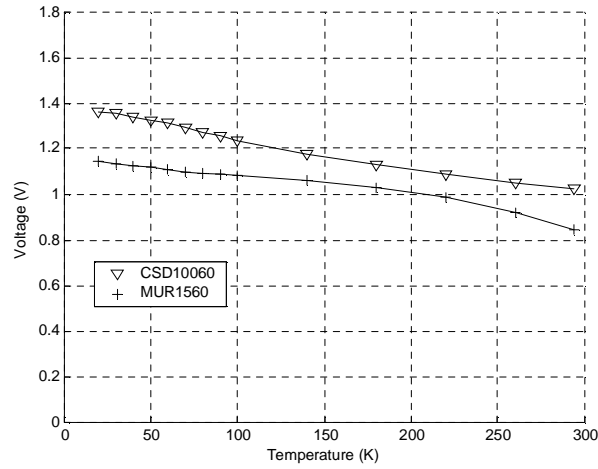


Figure 2-17 Measured diode on-state voltages at 2 A

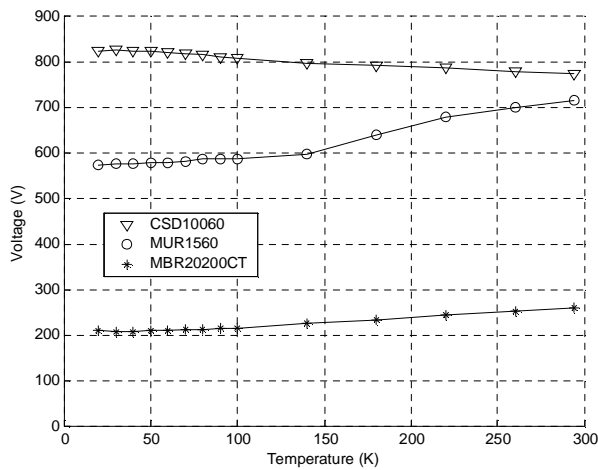


Figure 2-18 Measured diode breakdown voltages

2.5 Analysis of the semiconductor losses in the 120 V converters at low temperatures

The power converter was fabricated by screwing the MOSFET and diode onto a copper plate, 110×60 mm, for mounting onto the cold head. A PCB was used to form the power circuit and gate driver connections. The photograph of the prototype is shown in Figure 2-19.

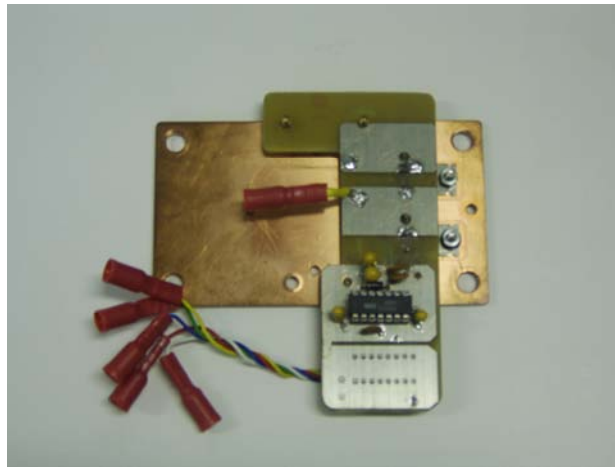


Figure 2-19 Single-transistor step-down converter prototype

Gate driving signals generated at room temperature were passed into the chamber via the signal feedthrough. The gate driver integrated circuit was located inside the chamber close to the semiconductor devices, but not in direct contact with the cold head. During the cryogenic experiments the minimum temperature of the driver integrated circuit was around 200 K, much higher than the cold head temperature.

Figure 2-20 shows the layout for the cryogenic experiments. The input and output power connections were passed into the cold chamber by the power feedthrough, which is on the left hand side of the cold chamber, Figure 2-20. Planar copper bus bars were used to reduce

parasitic circuit inductance between the feedthrough and the converter in the cold chamber. The input decoupling capacitors were located outside the chamber and beside the power feedthrough. The output filter was situated at room temperature next to the input capacitors. The signal feedthrough is on the right hand side of the cold chamber.



Figure 2-20 Prototype circuit inside the cold chamber

By configuring the converter with the input decoupling capacitors outside the cold chamber, the MOSFET and diode currents and voltages could be easily measured outside the chamber. A LeCroy current probe was used to measure the currents. The switching losses were obtained by multiplying switching frequency and the time integral of the device voltage and current products, whilst the on-state losses were calculated from a knowledge of the current, the static characteristics in Figures 2-11, 2-16 and 2-17 and the equations (2-42) and (2-43). The measured device losses were confirmed by measurement of the converter input and output powers using high resolution multimeters and measurement of the inductor losses.

$$P_{Cond_MOSFET} = I_{RMS}^2 R_{DS(on)} D \quad (2-42)$$

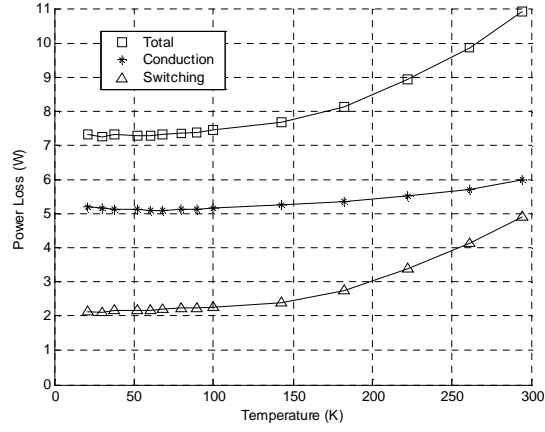
$$P_{Cond_Diode} = I_{AV} V_F (1 - D) \quad (2-43)$$

The cold head temperature was first decreased to 20 K and then increased to room temperature. During the warming process measurements were taken at a set of temperature points, every 10 K from 20 K to 100 K and every 40 K from 100 K to 300 K, taking care to ensure that thermal equilibrium had been reached inside the chamber at each temperature point.

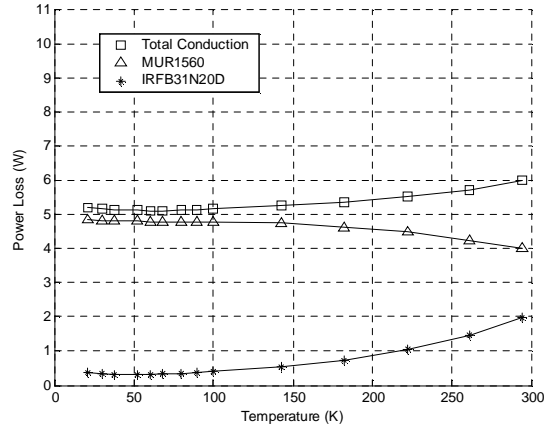
2.5.1 120 V buck converter with an ultrafast diode

Figure 2-21 (a) plots the total semiconductor losses in the step-down converter with the MUR1560 ultrafast diode in the temperature range 20-300 K, along with the conduction and switching losses. The losses in the individual devices are displayed in Figures 2-21 (b) and (c).

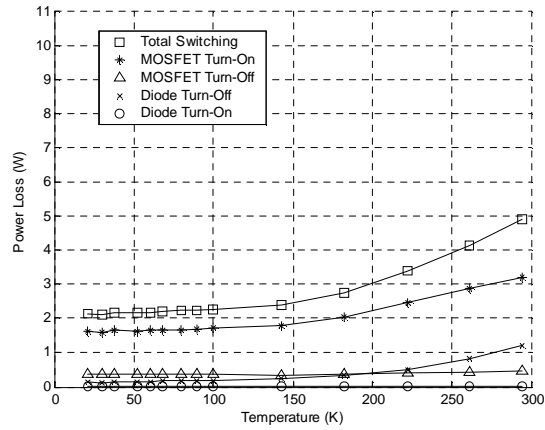
The total semiconductor loss decreases approximately by one-third at 20 K compared to the room temperature value, due to the reductions both in the conduction and switching losses, Figure 2-21 (a). The reduction in the switching loss is three times the reduction in the conduction loss across the temperature range, Figure 2-21 (a). The reduction in the IRFB31N20D MOSFET on-state loss is offset by the increase in the diode conduction loss, Figure 2-21 (b), the total conduction loss decreases by one-sixth at cryogenic levels. The total switching loss decreases by 60 % over the range 300-20 K, Figure 2-21 (c), which is largely due to the reduction in the diode reverse recovery. To illustrate the improvement in diode reverse recovery, the diode turn-off currents are plotted in Figure 2-22, where the peak reverse recovery current decreases by a factor of four, the reverse recovery time reduces by more than a half, and the reverse recovery charge drops by a factor of seven at 20 K compared to room temperature.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 2-21 Semiconductor losses in the buck converter with IRFB31N20D MOSFET, MUR1560 ultrafast diode

$$V_{In} = 120V, V_O = 60V, P_{Load} = 480W$$

The switching losses in the MOSFET and diode during the MOSFET turn-off transient are only a small proportion of the total switching loss at room temperature, moreover both vary little with temperature, remaining nearly constant in Figure 2-21 (c). In addition the MOSFET turn-on and turn-off intervals were found to decrease only slightly at low temperatures. The invariance of the MOSFET switching behaviour with temperature is in accordance with expectations based on the analysis in Section 2.2 and the measured variation in threshold voltage and transconductance, Section 2.4.1.

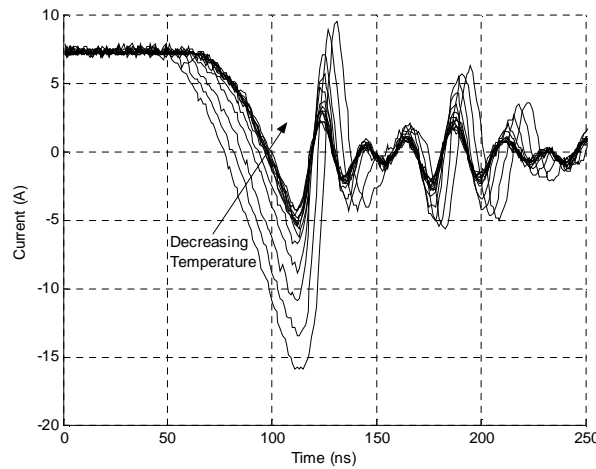
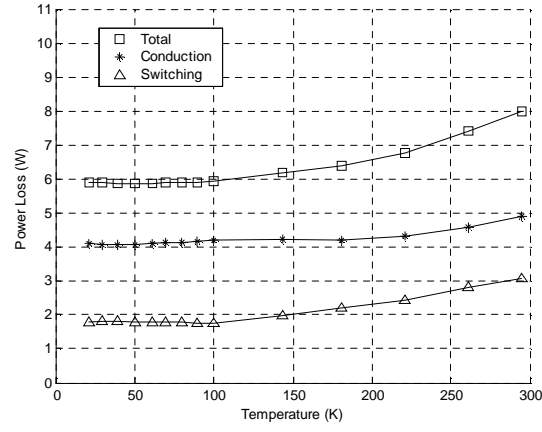


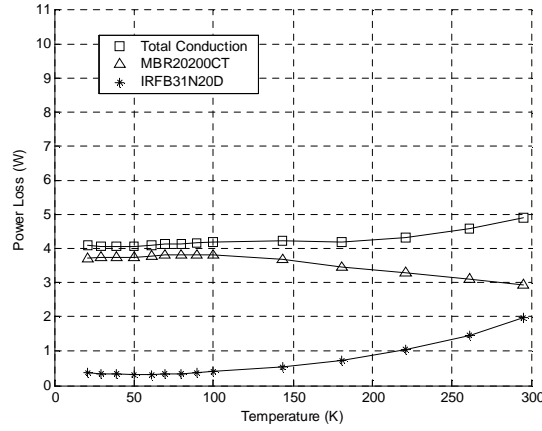
Figure 2-22 MUR1560 turn-off currents in the buck converter with IRFB31N20D MOSFET, $V_{In} = 120V$, $V_O = 60V$, $P_{Load} = 480W$
Temperature ranges from 20 K to 100 K in steps of 10 K
and from 100 K to 300 K in steps of 40 K

2.5.2 120 V buck converter with a Schottky diode

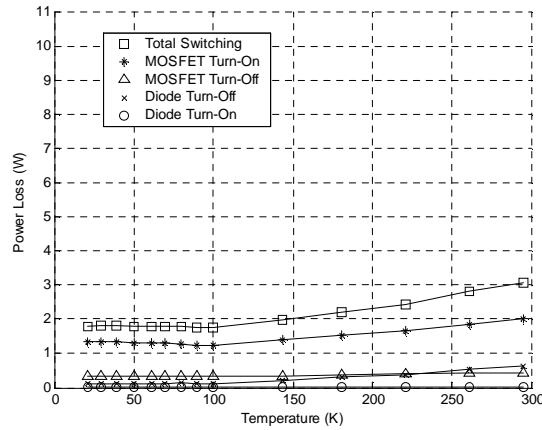
Figure 2-23 (a) plots the total semiconductor losses in the step-down converter with the MBR20200CT Schottky diode across the temperature range 20-300 K, together with the conduction and switching losses. The losses in the individual semiconductors are displayed in Figures 2-23 (b) and (c).



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 2-23 Semiconductor losses in the buck converter with IRFB31N20D MOSFET, MBR20200CT Schottky diode

$$V_{In} = 120V, V_O = 60V, P_{Load} = 480W$$

The total semiconductor loss decreases by one-fourth at 100 K due to the reductions both in the conduction loss and in the switching loss, Figure 2-23 (a). The losses remain approximately constant in the range 100-20 K.

The overall pattern of loss reduction at low temperatures is very similar to that seen with the P-i-N diode, however, the total losses are lower due to the superior characteristics of the Schottky diode at all temperatures. The conduction losses decrease by one-fifth in the temperature range 300-20 K, Figure 2-23 (b), resulting from the combined effects of the decreasing on-state loss in the MOSFET and the increasing conduction loss in the diode. The principal contribution to the switching loss reduction is from the decrease both in the MOSFET turn-on loss and in the diode turn-off loss, Figure 2-23 (c), which results in the total switching loss at cryogenic levels reducing by more than one-third compared to room temperature. The other two components of switching loss vary little across the temperature range.

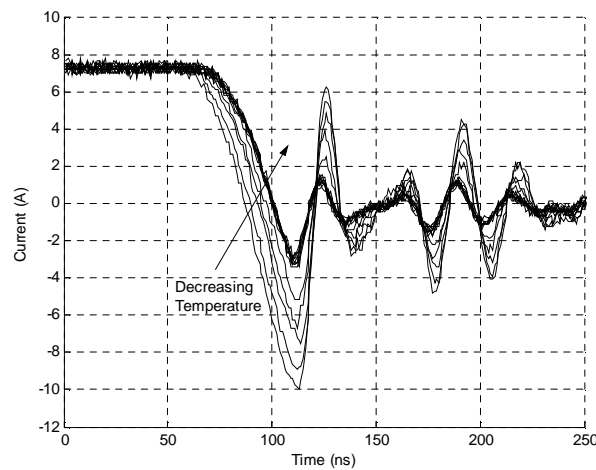


Figure 2-24 MBR20200CT turn-off currents in the buck converter with
IRFB31N20D MOSFET, $V_{In} = 120V$, $V_O = 60V$, $P_{Load} = 480W$
Temperature ranges from 20 K to 100 K in steps of 10 K
and from 100 K to 300 K in steps of 40 K

The decrease in the switching loss is due to the improvement in the diode reverse recovery at low temperatures, since the MOSFET switching properties change only slightly at low temperatures. Figure 2-24 plots the diode turn-off current at all temperatures. The peak reverse recovery current drops by 70 %, the reverse recovery time decreases almost by half and the reverse recovery charge reduces by a factor of three over the range 300-20 K.

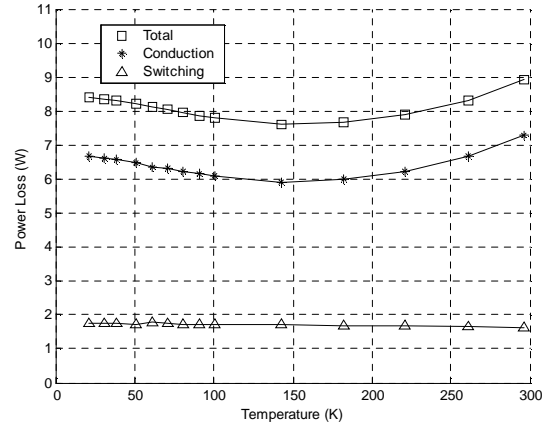
Theoretically, the Schottky diode has no reverse recovery, however as explained in Section 1.3.1 the presence of the p^+ guard ring creates a $p-n$ junction in parallel with the Schottky junction [2-14] and this is responsible for the reverse recovery behaviour.

2.5.3 120 V buck converter with a silicon carbide Schottky diode

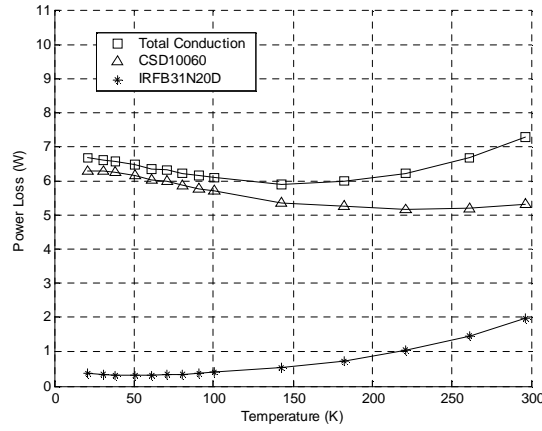
Figure 2-25 (a) plots the total semiconductor losses in the buck converter with the silicon carbide diode, CSD10060, over the temperature range 20-300 K, along with the conduction and switching losses. Figures 2-25 (b) and (c) display the losses in individual devices.

The total semiconductor loss has a minimum at approximately 140 K, Figure 2-25 (a). The variation in loss with temperature is determined by the conduction loss since the switching loss changes little. At higher temperatures the conduction loss falls with a drop in temperature due to the reduction in MOSFET resistance, however, at lower temperatures the increasing diode voltage dominates and the overall loss rises.

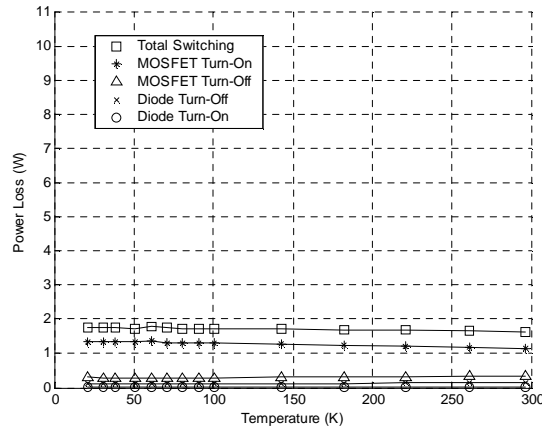
The switching losses, Figure 2-25 (c), have no significant variation across the temperature range. The SiC diode turn-off currents are plotted in Figure 2-26 at temperatures of 20 K, 60 K 100 K and 300 K. No apparent change is found either in the reverse recovery current or in the reverse recovery time. The MOSFET switching losses are again consistent with analysis in Section 2.2 and the measured variation in threshold voltage and transconductance at low temperatures Section 2.4.1.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 2-25 Semiconductor losses in the buck converter with IRFB31N20D MOSFET, CSD10060 silicon carbide diode
 $V_{In} = 120V, V_O = 60V, P_{Load} = 480W$

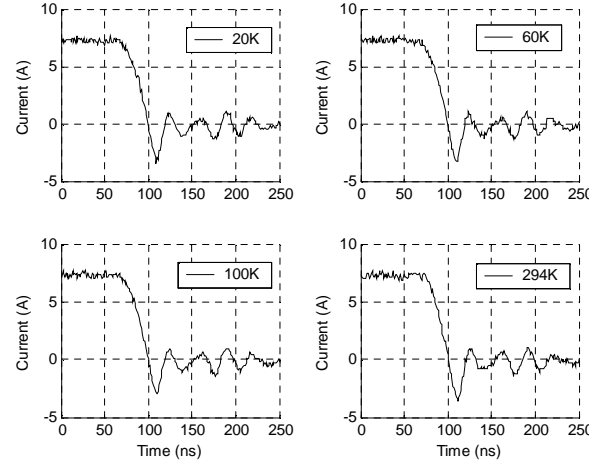


Figure 2-26 CSD10060 turn-off currents in the buck converter with IRFB31N20D MOSFET, $V_{In} = 120V$, $V_O = 60V$, $P_{Load} = 480W$

2.5.4 Summary of the semiconductor losses in the 120 V converters

Figure 2-27 summarises the total semiconductor losses in the three 120 V converters delivering 480 W to a 60 V load, whilst Figures 2-28 and 2-29 show the breakdown of total semiconductor loss into conduction and switching losses respectively. The total semiconductor loss for the prototypes with the silicon diodes has positive temperature coefficient, Figure 2-27, due to the reductions both in conduction and in switching losses at low temperatures [2-17]. There are significant reductions in the switching loss for both prototypes, Figure 2-29, due to the improved diode reverse recovery at low temperatures [2-17]; however, the reduction in conduction losses is limited by the increase in the diode on-state losses, Figure 2-28.

The SiC-diode based prototype shows the worst performance at low temperatures due to the large on-state voltage of the SiC diode. The increase in the SiC diode on-state loss outweighs the reduction in the MOSFET conduction loss at cryogenic temperatures and the total semiconductor loss at 20 K is only slightly lower than that at room temperature, Figure 2-27, however, the switching loss is the smallest of the three circuits and changes little with temperature, Figure 2-29.

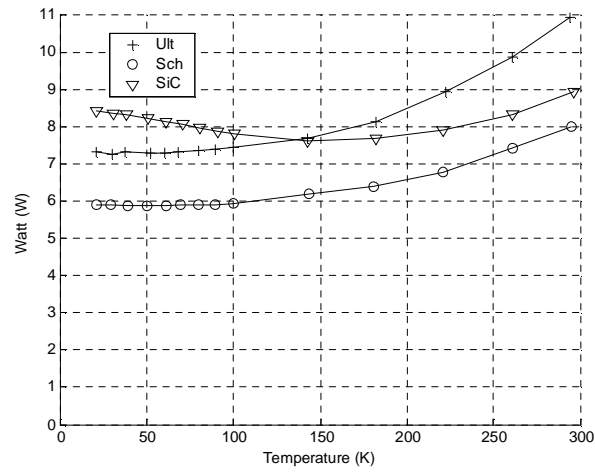


Figure 2-27 Semiconductor losses in the 120/60 V, 480 W single-transistor prototypes

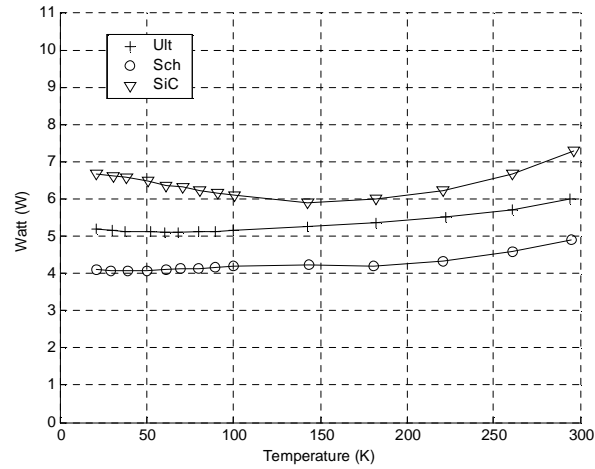


Figure 2-28 Conduction losses in the 120/60 V, 480 W single-transistor prototypes

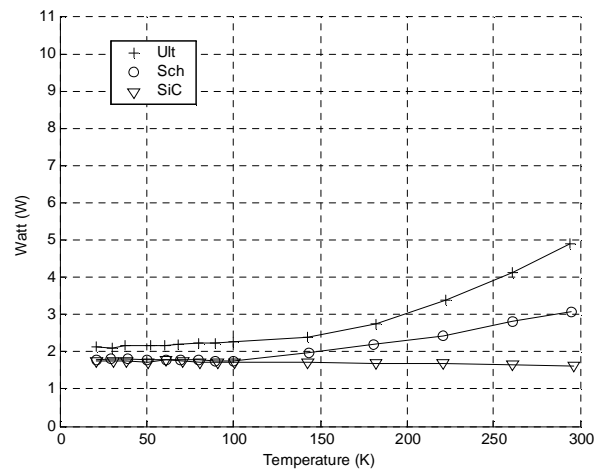


Figure 2-29 Switching losses in the 120/60 V, 480 W single-transistor prototypes

Operating the converters with a different transistor duty ratio will have little effect on the switching losses, however, the distribution of the conduction loss between MOSFET and diode will change leading to a different variation in overall loss with temperature. For example with a larger duty ratio the reduction in overall losses at low temperature will be greater.

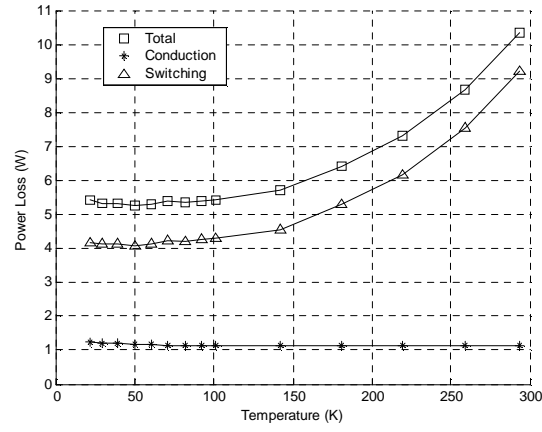
2.6 Analysis of the semiconductor losses in the 500 V converters at low temperatures

Two buck converters were built using the SPP20N60C3 MOSFET and either the ultrafast diode, MUR1560, or the silicon carbide diode, CSD10060. Both prototypes were operated from a 500 V supply and delivered 500 W to a 250 V load, the switching frequency being 50 kHz.

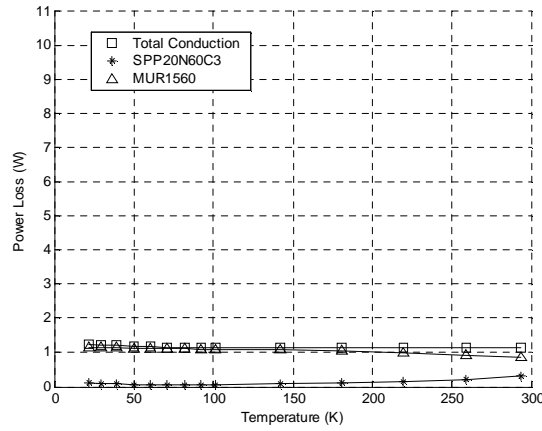
2.6.1 500 V buck converter with an ultrafast diode

Figure 2-30 (a) plots the total semiconductor losses, the conduction and switching losses, in the temperature range 20-300 K for the converter using the MUR1560 ultrafast diode. The losses in the individual semiconductors are displayed in Figures 2-30 (b) and (c).

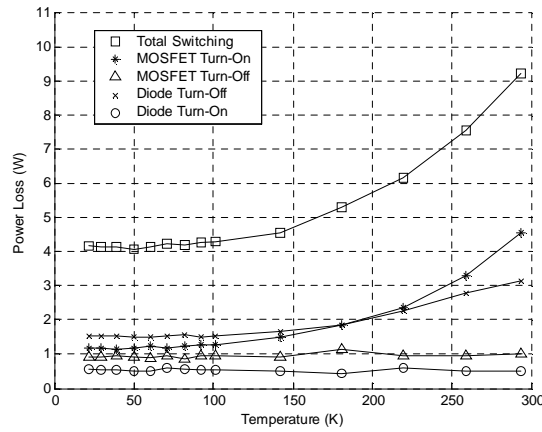
The total semiconductor loss decreases approximately by a factor of two with a decrease in temperature from 300 K to 20 K, Figure 2-30 (a), principally due to the 55 % reduction in the switching loss; the conduction loss changes little across the temperature range and only contributes a small proportion of the total semiconductor loss due to the reduced current level in the 500 V prototypes.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 2-30 Semiconductor losses in the buck converter with SPP20N60C3 MOSFET, MUR1560 ultrafast diode
 $V_{In} = 500V, V_O = 250V, P_{Load} = 500W$

The MOSFET turn-on loss decreases by a factor of four and the diode turn-off loss reduces by a half, Figure 2-30 (c), both contributing to the significant reduction in the total switching loss at 20 K. The other two components of switching loss have small proportions at room temperature and change little with temperature. The large reduction in the switching loss is mainly attributed to the improved diode reverse recovery at low temperatures. The MUR1560 turn-off currents at 500 V are plotted at temperatures of 20 K, 60 K, 100 K and 300 K in Figure 2-31, where the peak reverse recovery current decreases by 60 %.

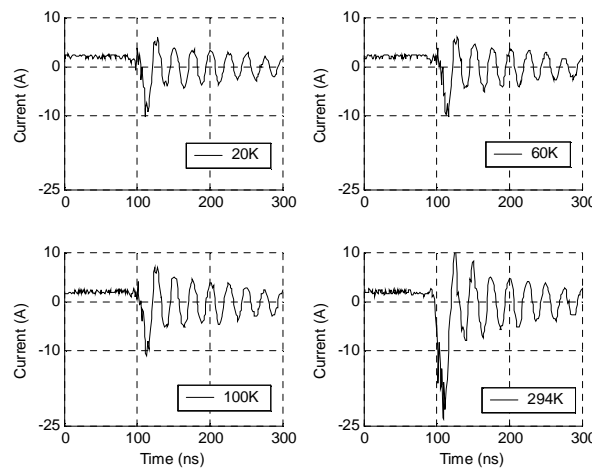
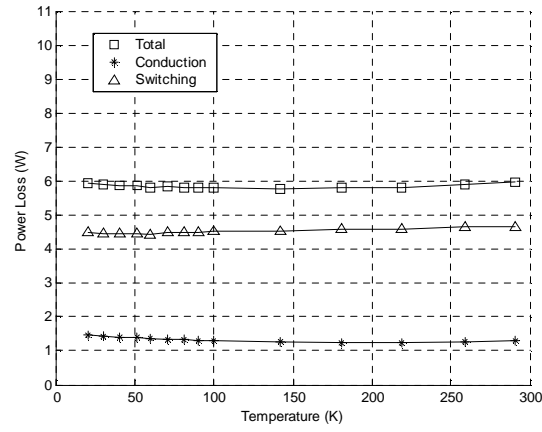


Figure 2-31 MUR1560 turn-off currents in the buck converter with SPP20N60C3 MOSFET, $V_{in} = 500V$, $V_O = 250V$, $P_{Load} = 500W$

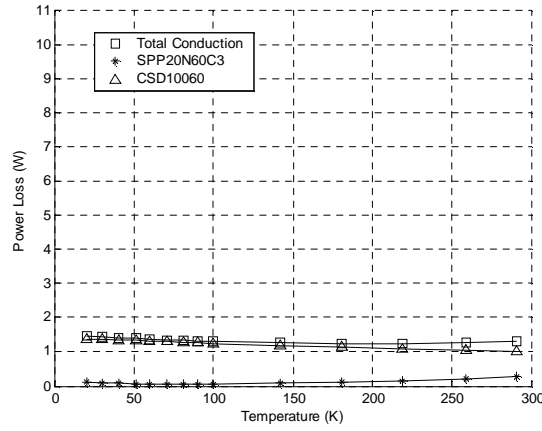
2.6.2 500 V buck converter with a silicon carbide Schottky diode

Figure 2-32 (a) plots the conduction loss, switching loss and sum of the two over the temperature range 20-300 K for the SiC-diode (CSD10060) based prototype. Figures 2-32 (b) and (c) display the losses in the individual semiconductor devices.

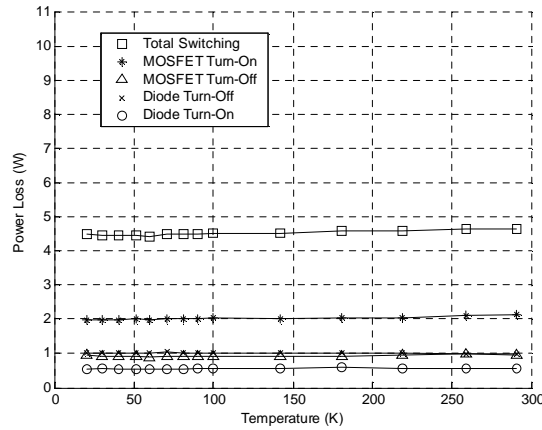
The total semiconductor loss changes little with temperature, Figure 2-32 (a). The switching loss dominates, accounting for nearly 80 % of the total loss, and remains approximately constant over the temperature range. The conduction loss shows a small increase at very low temperatures, Figure 2-32 (a), due to the higher diode on-state voltage.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 2-32 Semiconductor losses in the buck converter with SPP20N60C3 MOSFET, CSD10060 silicon carbide diode

$$V_{In} = 500V, V_O = 250V, P_{Load} = 500W$$

The SiC diode turn-off currents are plotted in Figure 2-33 at four temperatures, 20 K, 60 K, 100 K and 294 K, where no appreciable change is observed either in the reverse recovery current or in the reverse recovery time.

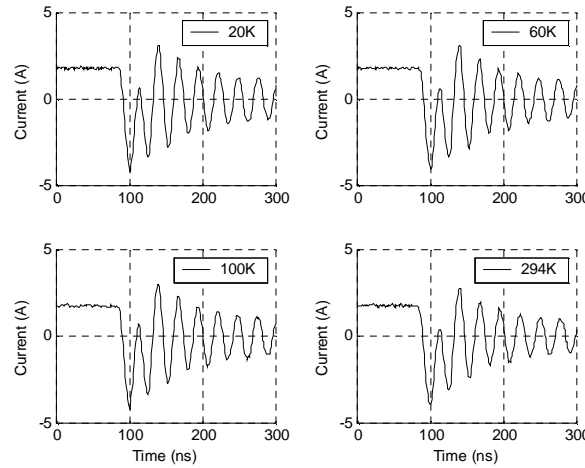


Figure 2-33 CSD10060 turn-off currents in the buck converter with SPP20N60C3 MOSFET, $V_{in} = 500V$, $V_O = 250V$, $P_{Load} = 500W$

2.6.3 Summary of semiconductor losses in the 500 V converters

Figure 2-34 plots the total semiconductor losses and switching losses for the 500 V prototypes. The SiC-diode based converter yields relatively small losses at higher temperatures and below 140 K it loses the advantage. The switching loss dominates the total semiconductor loss for both prototypes. It decreases by over a half at 20 K in the ultrafast diode based prototype whilst in the SiC prototype it is constant across the temperature range. The conduction losses are not displayed since they are relatively small.

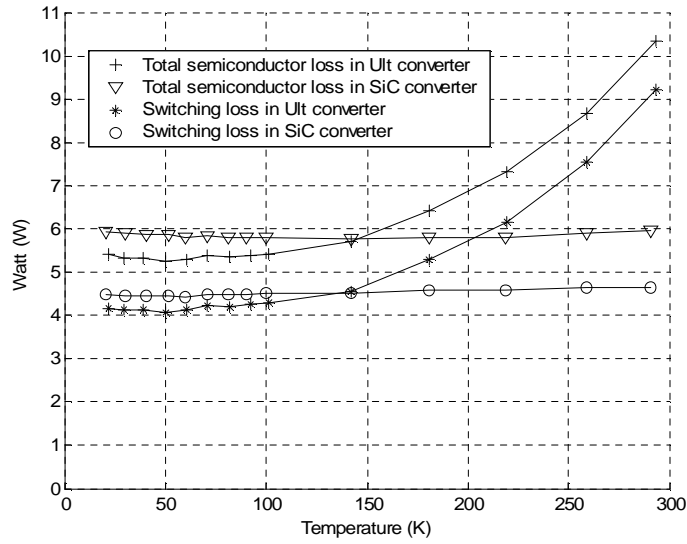


Figure 2-34 Semiconductor losses in the 500/250 V, 500 W single-transistor prototypes

2.7 Conclusions

- The on-state resistance of the IRFB31N20D MOSFET drops by a factor of six at 50 K, and the breakdown voltage decreases by 23 %. The SPP20N60C3 CoolMOS device has a lower on-state resistance at room temperature than conventional high-voltage MOSFETs with the same die size; however the proportionate decrease of resistance at low temperature is slightly less significant than that in the lower voltage device, attributed to the CoolMOS structure. The breakdown voltage of the SPP20N60C3 shows a similar decrease at low temperature to that in the IRFB31N20D.
- The reduction in the total semiconductor losses at cryogenic temperatures was limited by the increase in diode conduction losses.
- The MOSFET switching characteristic has very little improvement at low temperatures. No appreciable variation was observed in the switching speed,

which was consistent with the static measurement of threshold voltage and transconductance.

- Large reductions in the switching losses related to diode reverse recovery were observed in the silicon diode prototypes at low temperature, however, reverse recovery effect remained a significant source of loss. No reverse recovery effects were noticeable in the SiC diode based prototype.
- The prototype performance at low temperature could be further improved by placing the input capacitor inside the cold chamber to reduce the stray inductance and associated losses.

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Chapter 3

Cryogenic operation of two-transistor step-down converters

This Chapter investigates the semiconductor losses over the temperature range 20-300 K in two types of DC-DC step-down converter formed by two MOSFETs: one being a synchronous rectifier operating from 120 V and 500 V DC supplies, and the second a soft-switching buck converter operating from a 120 V DC supply. The semiconductor losses in these prototypes are compared with those in the single-transistor step-down converters presented in the last Chapter. The objective is to examine ways of improving converter efficiency at cryogenic temperatures, in particular by eliminating diode conduction, diode reverse recovery and transistor switching losses.

3.1 Synchronous rectifier

The single-transistor step-down converter discussed in Chapter 2 employs a diode to freewheel the inductor current when the transistor is in the off-state. The diode on-state voltage can limit the conversion efficiency, especially for very low converter output voltages. However, even using Schottky diode technology, physical limitations prevent the diode forward voltage from being reduced below around 0.3 V [3-1]. On the other hand the on-state resistance of a MOSFET can be lowered almost without limit either by increasing the die size or by paralleling discrete devices [3-1, 3-2].

Furthermore, the limitation on circuit performance imposed by diode voltage drop becomes more significant at low temperatures since the diode on-state voltage tends to increase whilst the on-state resistance of a MOSFET falls. The potential benefits of operating a converter at very low temperatures may therefore be limited by the behaviour of the diodes.

One approach to overcoming this problem is the synchronous rectifier technique, which has been developed in recent years for very low output voltage switched-mode power supplies, typically output voltages less than 3 V. The synchronous rectifier technique involves replacing the freewheel diode by a low voltage MOSFET as shown in the step-down converter in Figure 3-1. S_1 is the switching transistor that determines the converter output voltage whilst S_2 is the synchronous rectifier. When S_1 turns off the inductor current will tend to freewheel through the body diode of S_2 , however, if S_2 is switched on, reverse conduction will occur through the channel, diverting current away from the body diode, providing that the on-state resistance of S_2 is sufficiently low. Reverse current flow through the MOSFET channel can occur since the device operates by majority carrier conduction.

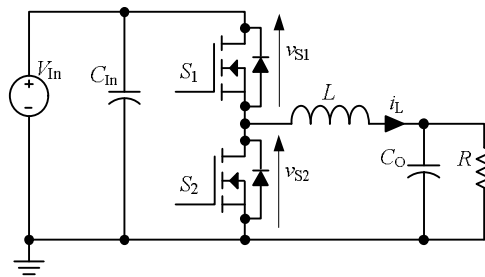


Figure 3-1 Step-down converter with synchronous rectifier

To illustrate the principle, the forward $i - v$ characteristics are compared in Figure 3-2 of the IRFB31N20D MOSFET and a fast recovery rectifier 1N3891 ($V_{BD} = 200V, I_{AV} = 12A$) with the model provided by [3-3]. It is seen that in this particular case the MOSFET voltage drop is lower than that of the diode for currents up to approximately 12 A, resulting in lower conduction losses.

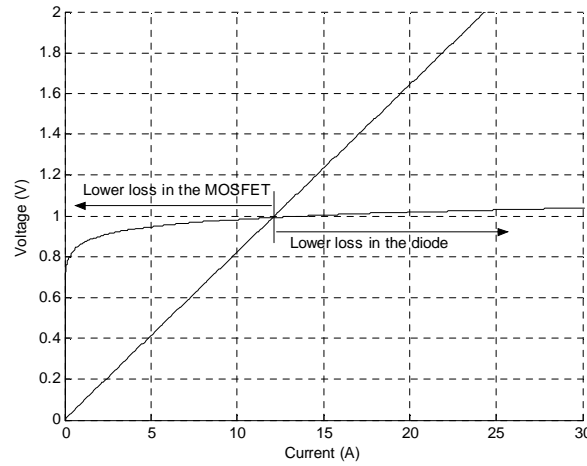


Figure 3-2 Forward voltage comparison of a synchronous rectifier and diode at 25°C

The relative temperature coefficients of diode on-state voltages and MOSFET on-state resistances suggest that the synchronous rectifier technique may offer significant benefits for cryogenic power conversion.

In the following sections two step-down DC-DC converter topologies that use synchronous rectifiers are examined at low temperatures. The first circuit uses a hard-switching synchronous rectifier operating from 120 V and 500 V DC supplies, whilst in the second the synchronous rectifier is soft-switching operating from 120 V.

3.1.1 Synchronous rectifier design

The synchronous rectifier circuit was designed to operate from two voltage levels, 120 V and 500 V. The detailed design requirements are listed in Table 3-1, and are the same as those used for the single-transistor converters in Chapter 2.

The input capacitor, output filter inductor and capacitor were chosen based on the results of applying the design requirements to the equations (2-1), (2-2) and (2-3), resulting in the same passive component values as used in Chapter 2, Table 2-2. For the 120 V synchronous

rectifier circuit the MOSFET IRFB31N20D was chosen, and the MOSFET SPP20N60C3 was selected for the 500 V circuit. Both are the same as used in Chapter 2, Table 2-3.

Table 3-1 Synchronous rectifier design requirements

Design Parameters	Converter input voltage V_{In}	
	120 V	500 V
Input current (A)	4	1
Input power (W)	480	500
Output voltage (V)	60	250
Output current (A)	8	2
Duty ratio	50%	50%
Frequency (kHz)	50	50
Input voltage ripple (V)	6	25
Output voltage ripple (V)	0.6	2.5
Inductor current ripple (A)	1.2	0.3

Using the same passive components as in the single-transistor step-down converters, the synchronous rectifier was realised by replacing the freewheel diode with another power MOSFET. The control signals were generated at room temperature and transferred into the cold chamber via the signal feedthrough. An IR2110 level shifting gate driver integrated circuit was located inside the cold chamber next to the MOSFETs; however it was not in direct contact with the cold head. During testing its temperature did not fall below 200 K. The output filter, the input decoupling capacitor and filter were left at room temperature outside the cold chamber, allowing the individual device currents to be measured. Planar bus bars were used to minimise the stray inductance of the power circuit connections between the power devices and the feedthrough. Figure 3-3 displays the picture of the 120 V synchronous rectifier prototype, which was placed inside the cold chamber.

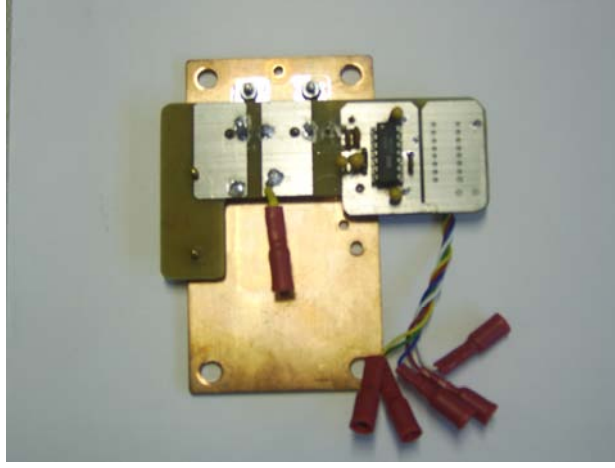


Figure 3-3 120 V synchronous rectifier prototype

3.1.2 Gate control strategy

Precise control is required for the two MOSFETs in the synchronous rectifier. To avoid shoot through, a dead time, T_{Dead} , is usually introduced between the turn-off of one device and the turn-on of the other, during which time the inductor current is carried through the body diode of the MOSFET S_2 in Figure 3-1. To analyse the dead time operation, Figure 3-4 plots the schematic waveforms of the individual MOSFET gate-source voltages and the current commutation during the switching transients.

When the S_1 gate voltage, v_{GS1} , drops from the plateau value during the turn-off process, Figure 3-4 (a), the inductor current begins commutating from S_1 to the S_2 body diode until v_{GS1} falls to the threshold voltage V_T at the end of period T_1 , Figure 3-4 (a). During the interval T_2 , v_{GS1} decreases to zero and S_1 is in the off-state, the inductor current flows through the S_2 body diode. A short duration of dead time, T_{Dead} , is then inserted during which no driving signal is applied to either MOSFET, and the inductor current continues freewheeling through the body diode of S_2 . At the end of T_{Dead} the gate-source voltage is applied to S_2 , but no current flows through S_2 until v_{GS2} rises to V_T at the end of period

T_3 . v_{GS2} increases from V_T during interval T_4 , whilst the inductor current is diverted from the S_2 body diode to the channel. There is no plateau period in v_{GS2} since the drain source voltage is already zero.

Figure 3-4 (b) plots the transient in which the inductor current commutates from S_2 back to S_1 . During the interval T_5 , Figure 3-4 (b), v_{GS2} decreases to V_T whilst the channel current diverts to the body diode. At the start of interval T_6 the body diode takes over the inductor current completely. The current then freewheels through the body diode until the end of period T_7 when v_{GS1} increases to V_T . During T_8 the inductor current commutates from the S_2 body diode to S_1 whilst v_{GS1} increases from V_T to the plateau value.

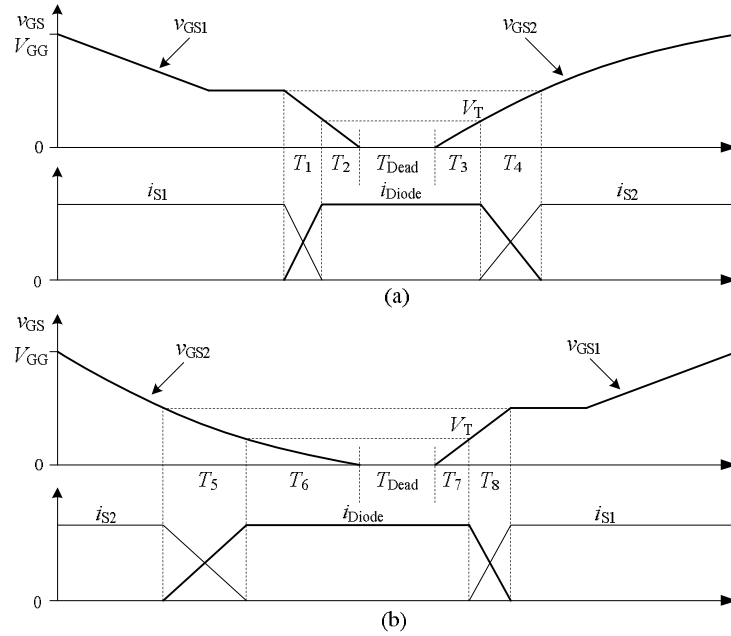


Figure 3-4 MOSFET switching waveforms: (a) turn-off of S_1 and turn-on of S_2 , (b) turn-off of S_2 and turn-on of S_1 ; i_{S1} : current through S_1 ; i_{S2} : current through S_2 ; i_{Diode} : current through the body diode of S_2

Examination of Figure 3-4 shows that the S_2 gate-source voltage waveform is different to that of S_1 , principally due to the operation in the third quadrant of the i_D, v_{DS} plane. The conduction of the S_2 body diode prior to the channel results in zero voltage switching, during which the drain-source voltage of S_2 is virtually zero. Therefore there is no charge flow through the Miller capacitance. As a result the plateau region of the S_2 gate voltage plot is not visible, the waveform shows an exponential charging and discharging of the input capacitor [3-4], Figure 3-4.

The conduction of the body diode has two drawbacks, increased conduction loss due to the larger on-state voltage, and increased switching losses due to the body diode reverse recovery during the S_1 turn-on transient. Both decrease the converter efficiency and limit the application of the synchronous rectifier to low voltage levels [3-4]. To decrease the body diode conduction, the dead time may be decreased and the gate-source voltages for both MOSFETs are even overlapped, providing that the instant when v_{GS} of the out-going MOSFET falls below V_T occurs before v_{GS} of the incoming MOSFET increases to V_T [3-5].

To illustrate how this improves the switching waveforms, Figure 3-5 plots the amplitude of the measured peak reverse recovery current through the S_2 body diode with different dead times for the 120 V synchronous rectifier at room temperature supplying 60 V output to a 480 W load. The dead time is defined as the time interval between the instant of the gate-source voltage approaching zero for S_2 and rising from zero for S_1 . A 4 Ω gate resistor was used to control the S_1 switching speed. The peak reverse recovery current has a minimum value of 10.8 A at -40 ns, Figure 3-5, where the negative sign implies that the two driving signals are overlapping. The minimum peak reverse current is less than half the value that is measured with a dead time of 50 ns. Further decreases in the dead time below -40 ns may result in shoot through and thereby increase the current. The S_2 turn-off currents are plotted in Figure 3-6 with dead times of 50 ns and -40 ns respectively at room temperature.

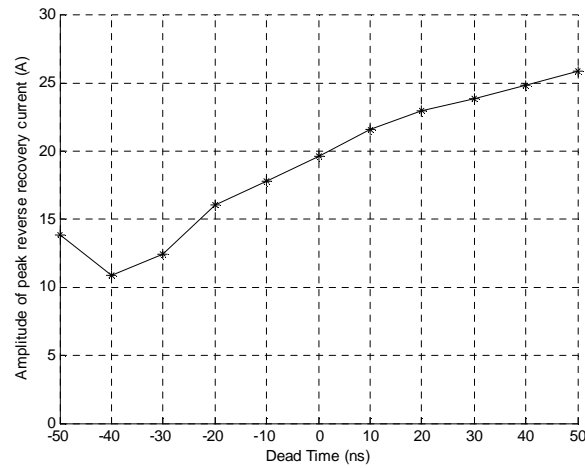


Figure 3-5 Amplitude of peak reverse current against dead time in the 120 V synchronous rectifier at 20°C with a 60 V, 480 W output

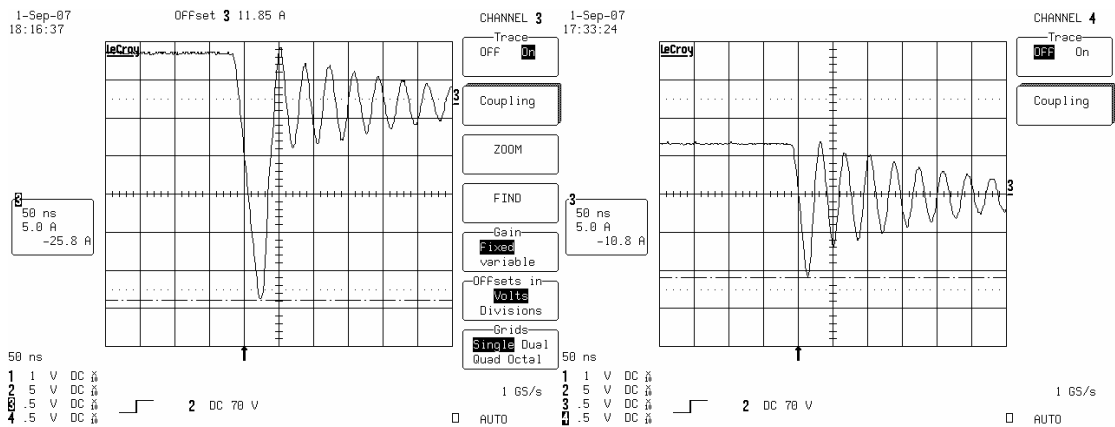


Figure 3-6 S_2 turn-off currents with dead time of 50 ns (left) and -40 ns (right) at 20°C for the 120 V synchronous rectifier with a 60 V, 480 W output

The optimum value of dead time is dependent on the gate threshold voltage of the MOSFETs and will therefore vary with temperature. At reduced temperature the increase in gate threshold voltage will require further reductions in the dead time to minimise switching losses. The threshold voltage of the IRFB31N20D at low temperature examined in Chapter 2 is re-plotted in Figure 3-7 with that of SPP20N60C3. Both increase by more than 1 V at temperatures down to 20 K. When the circuit was tested at low temperatures the dead time was adjusted at each temperature to minimise the peak reverse recovery current through the

S_2 body diode. Due to limitations of the number of pins on the feedthrough, it was not possible to measure the individual gate-source voltages and the actual dead times that were used, however, the dead time was reduced at low temperatures by approximately 10 ns.

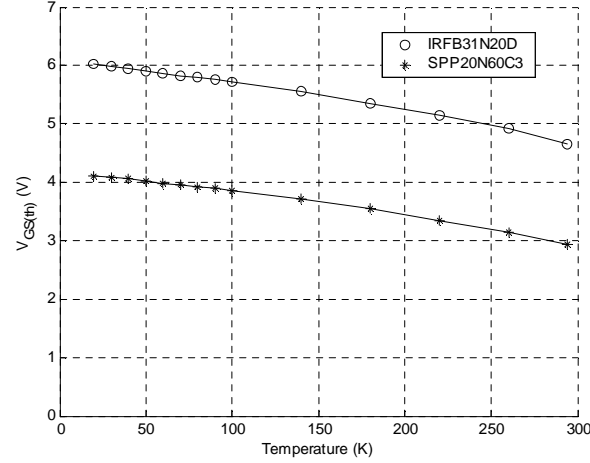


Figure 3-7 Gate threshold voltages, $V_{GS} = V_{DS}, I_D = 250\text{mA}$

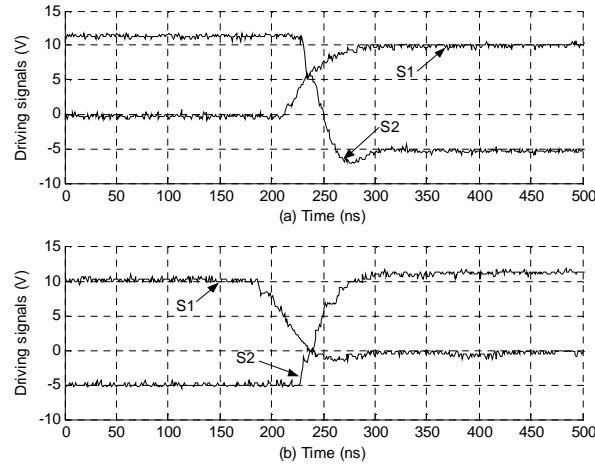


Figure 3-8 Gate-source voltages for the 120 V synchronous rectifier at 20°C: (a) turn-off of S_2 and turn-on of S_1 , (b) turn-off of S_1 and turn-on of S_2

To protect against false turn-on of S_2 which may occur due to current injected into the gate through the gate-drain capacitance as the drain voltage rises rapidly, a negative bias of -5 V was placed on the gate-source in the off-state. Figure 3-8 plots the driving signals for the 120 V synchronous rectifier, where the S_2 driving signal has -5 V off-state level. The dead time is set at -40 ns during the S_2 turn-off and S_1 turn-on interval, Figure 3-8 (a). During S_1

turn-off and S_2 turn-on transient, the dead time has little effect on the switching waveforms and it was set to zero, Figure 3-8 (b).

3.1.3 Semiconductor losses at room temperature

Before testing the circuits at low temperature, the losses were first examined at room temperature and compared with design predictions. The circuit operated from a 120 V source at 50 kHz and delivered 480 W at 60 V to the load. The MOSFET parameters are the same as used in Chapter 2, Table 2-5.

The MOSFET drain-source voltage and drain current during the individual switching intervals were calculated using the equations (2-20), (2-21), (2-26) to (2-33), (2-35) and (2-36) from Chapter 2. Considering the stray inductance and the output capacitor of the other MOSFET, L_D was increased to 80 nH and the output capacitance was increased to 340 pF. The switching losses were calculated by time integration of the current and voltage products multiplied the switching frequency and are listed in Table 3-2 for both MOSFETs, along with the measured switching losses in the 120 V synchronous rectifier at room temperature.

Table 3-2 Calculated and measured switching losses in the 120 V synchronous rectifier at 20°C

Switching loss	Units	Calculated	Measured
S_1 turn-on	W	0.27	0.74
S_1 turn-off	W	0.76	0.34
S_2 turn-on	W	0	0.04
S_2 turn-off	W	0.58	0.44

The predicted and measured switching waveforms are plotted in Figure 3-9 for S_1 . There is a large pulse of forward current through S_1 at turn-on in the measured waveform due to the reverse recovery of the S_2 body diode, which was thought to account for the large difference

in the predicted and measured S_1 turn-on losses. The difference in the S_1 turn-off losses between the predicted and measured values may be caused by the piecewise linear approximation for the MOSFET non-linear gate-drain capacitance. In particular when S_1 turns off, the voltage across S_2 falls and the S_2 capacitance will rise; however, this effect is not included in the calculations. Since the conduction of S_2 body diode prior to the channel ensures the zero-voltage turn-on, the S_2 turn-on loss is calculated as zero. The measured turn-off loss in S_2 is due to the reverse recovery of the S_2 body diode. The oscillations in the measured waveforms at around 28 MHz were attributed to the stray inductance ringing with device capacitance. The natural frequency of the stray inductance (80 nH) and the MOSFETs drain-source capacitance (340 pF) is 32 MHz.

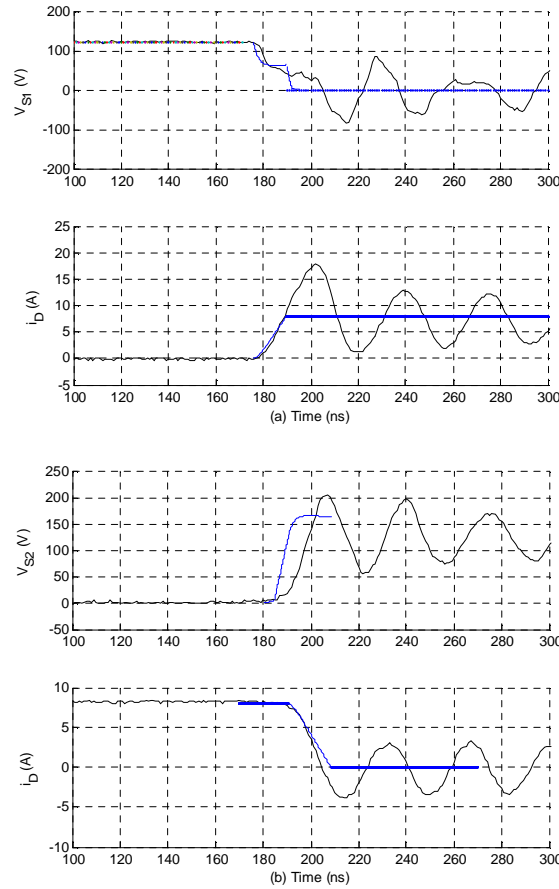


Figure 3-9 Predicted and measured S_1 switching waveforms: (a) turn-on, (b) turn-off; blue: analytical results; black: measured waveforms

The measured conduction losses in the 120 V synchronous rectifier are compared with the values in the single-transistor buck converters at room temperature in Table 3-3. The conduction losses in the synchronous rectifier circuit reduce by 18 %, 33 % and 45 % compared with the values in the single-transistor converters with the Schottky, ultrafast and SiC diodes respectively.

Table 3-3 Measured conduction losses in the 120 V prototypes at 20°C

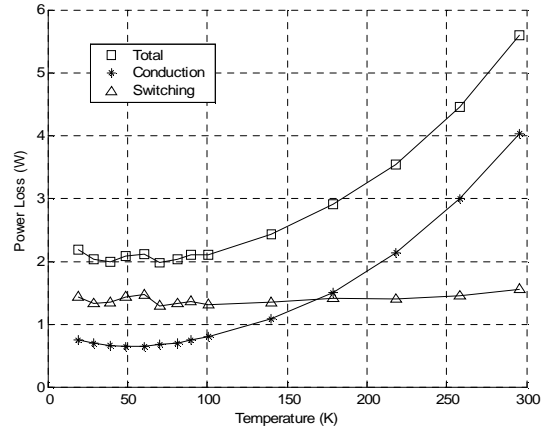
Semiconductor loss	Syn	Sch	Ult	SiC
Conduction losses (W)	4.01	4.92	6.00	7.31

3.1.4 Analysis of the semiconductor losses in the synchronous rectifiers at low temperatures

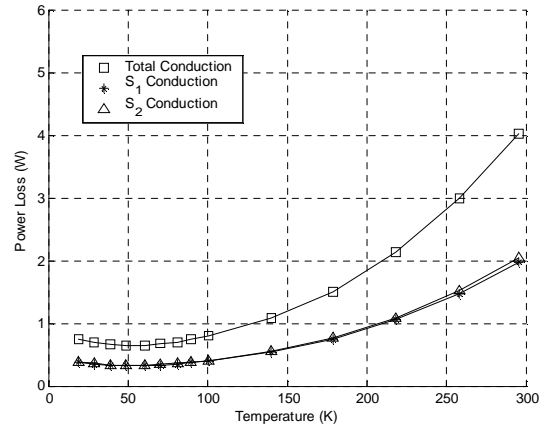
The synchronous rectifier was examined across the temperature range 20-300 K. Using the same layout as in Chapter 2, the currents and voltages for each MOSFET were measured outside the cold chamber. The switching losses were obtained by multiplying the switching frequency by the time integral of the device voltage and current products, whilst the on-state losses were calculated from a knowledge of the current, the static characteristic in Figure 2-11, and using the equation (2-42). The measured device losses were also confirmed by measurement of the inductor losses and the converter input and output powers using high resolution multimeters.

3.1.4.1 120 V synchronous rectifier

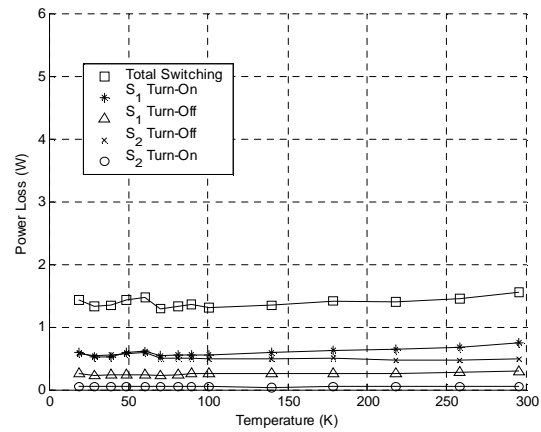
Figure 3-10 (a) plots the semiconductor losses in the 120 V synchronous rectifier across the temperature range 20-300 K and Figures 3-10 (b) and (c) display the losses in the individual semiconductor devices, where the prototype operated with the optimised dead time at all temperatures.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 3-10 Semiconductor losses in the synchronous rectifier with two IRFB31N20D MOSFETs, $V_{In} = 120V$, $V_O = 60V$, $P_{Load} = 480W$

The total semiconductor loss at cryogenic temperatures is approximately one-third of the room temperature value, Figure 3-10 (a), which is due to the significant reduction in the conduction loss. Both MOSFETs have the same on-state losses due to the approximately equal conducting durations, and the total conduction loss at 50 K is approximately 16 % of the room temperature value, Figure 3-10 (b). However, the switching loss changes little over the temperature range, Figure 3-10 (a) and (c). The S_2 turn-off currents are plotted in Figure 3-11 at temperatures of 20 K, 60 K, 100 K and 294 K. No apparent reduction is observed either in the reverse recovery current or in the reverse recovery time, except that the ringing amplitude decreases at low temperatures.

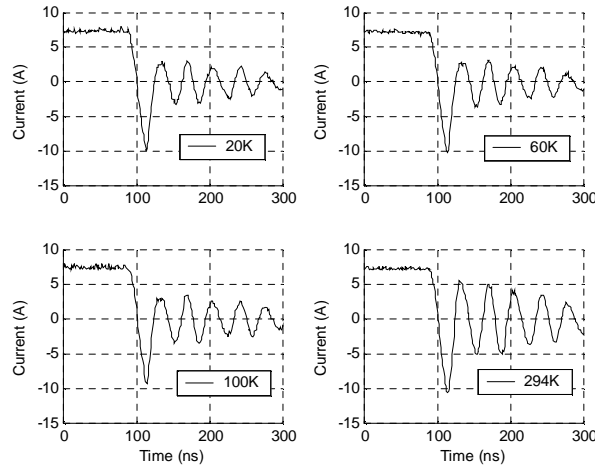
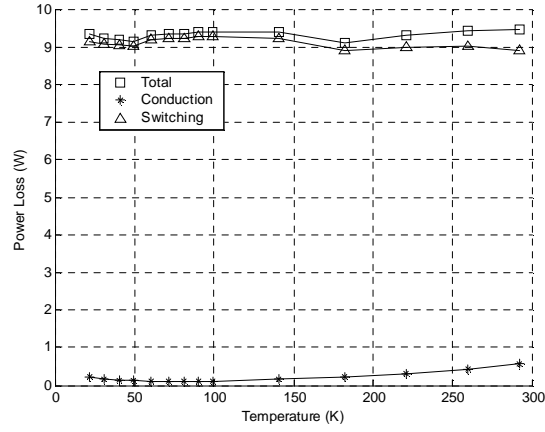


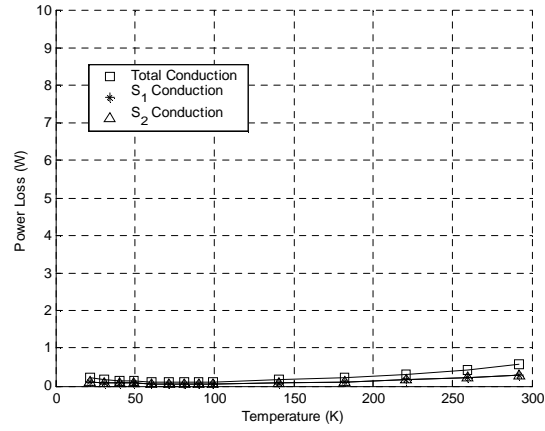
Figure 3-11 S_2 turn-off currents in the synchronous rectifier with two IRFB31N20D MOSFETs, $V_{In} = 120V$, $V_O = 60V$, $P_{Load} = 480W$

3.1.4.2 500 V synchronous rectifier

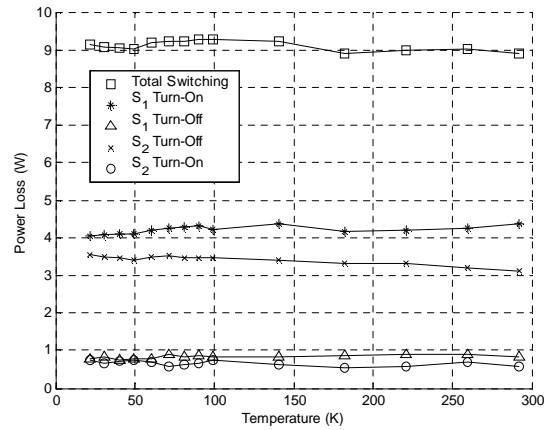
Figure 3-12 (a) displays the total semiconductor losses, conduction and switching losses in the synchronous rectifier operating from a 500 V source over the temperature range 20-300 K. The circuit used two SPP20N60C3 devices. The losses in the individual semiconductor devices are plotted in Figures 3-12 (b) and (c). The prototype operated with the dead time adjusted to minimise the peak reverse recovery current of the S_2 body diode at each temperature. The dead time was approximately -20ns. No gate resistors were added.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 3-12 Semiconductor losses in the synchronous rectifier with two SPP20N60C3 MOSFETs, $V_{In} = 500V$, $V_O = 250V$, $P_{Load} = 500W$

The total semiconductor loss is approximately constant across the temperature range, Figure 3-12 (a), due to the almost constant switching losses. Examination of the switching losses shows that all four components change little with temperature, Figure 3-12 (c). Although the on-state losses of both MOSFETs decrease with a decrease in temperature, Figure 3-12 (b), these losses are too small to make any difference to the total semiconductor loss.

Figure 3-13 displays the S_2 turn-off currents at temperatures of 20 K, 60 K, 100 K and 294 K. No appreciable change is found either in the reverse recovery current or in the reverse recovery time. Only the current ringing effect decreases dramatically at low temperatures.

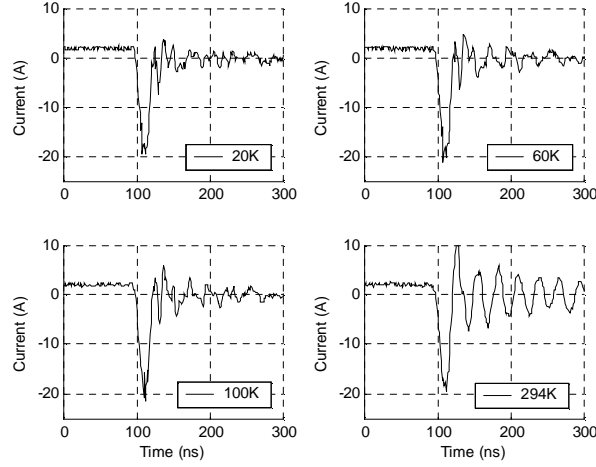


Figure 3-13 S_2 turn-off currents in the synchronous rectifier with two SPP20N60C3 MOSFETs, $V_{In} = 500V$, $V_O = 250V$, $P_{Load} = 500W$

3.2 Soft-switching buck converter

Although the synchronous rectifier offers a significant reduction in the conduction loss at low temperatures due to the diode-less configuration, the switching loss remains significant and is the dominant loss at low temperature in the results reported in the previous section. Moreover the residual switching loss is almost independent of temperature, Figure 3-10 and 3-12. Therefore, a soft-switching technology is desirable to diminish or eliminate the switching losses.

3.2.1 Soft-switching circuit selection

In broad terms there are two classes of soft switching techniques, those which create a natural current zero and enable device turn-off without loss, known as zero-current-switching (ZCS) circuits, and those which create a natural voltage zero to allow loss-less turn-on, known as zero-voltage-switching (ZVS) circuits [3-6]. ZCS circuits have the disadvantage that turn-on losses and diode reverse recovery losses remain, however, in ZVS circuits the remaining turn-off losses can be controlled by using capacitor snubbers.

A ZVS technique was chosen, and to enable straightforward implementation a circuit was selected which required a minimum of additional components and which did not increase the MOSFET off-state voltages, important due to the reduction in breakdown voltage at low temperatures. Therefore, a zero-voltage-switching clamped-voltage (ZVS-CV) topology was chosen as shown in Figure 3-14. Only two additional snubber capacitors and a small filter inductor are required to modify the synchronous rectifier circuit in Section 3.1. The ZVS-CV technique employs a resonant-transition during the switching interval of short but finite duration to realise zero voltage switching in both MOSFETs, and the off-state voltage of each MOSFET is clamped at the input voltage level [3-7]. Moreover, the ZVS-CV converter may still use the transistor duty ratio for output voltage control. The negative side is that the

conduction losses increase due to the increased ripple current level in the filter inductor. The inductor must be chosen such that the inductor current transiently reverses as described in the following section.

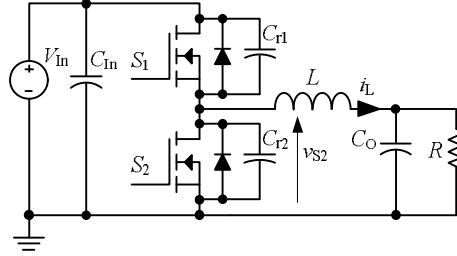


Figure 3-14 ZVS-CV soft-switching circuit

3.2.2 ZVS-CV circuit operation and design

The idealised circuit waveforms for a complete period are plotted in Figure 3-15. The waveforms show the gate-source voltages of the two MOSFETs, the drain-source voltage of S_2 , v_{s2} , and the inductor current i_L . A small dead time is present in the gate-source voltages and the inductor current is seen to have a large ripple component reversing for a short period of time. As a result, each MOSFET conducts in the reverse direction, either through the body diode or channel, immediately before conducting in the forward direction. Furthermore each transition of the v_{s2} waveform is initiated by the turn-off of one of the MOSFETs as described below.

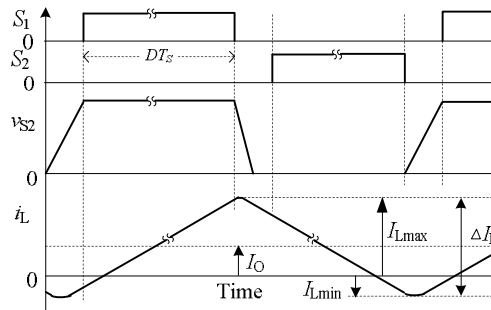


Figure 3-15 ZVS-CV ideal main waveforms

Figure 3-16 illustrates the positive-going transition of v_{s2} and the commutation of current from S_2 to S_1 . Figure 3-16 (a) shows that the inductor current i_L is initially carried by S_2 since the inductor current is now negative. After S_2 turns off the current is transferred to the snubber capacitors C_{r1} and C_{r2} , charging C_{r2} and discharging C_{r1} in a controlled manner, Figure 3-16 (b), and the voltage v_{s2} then rises to V_{in} from zero whilst the voltage across S_1 decreases from V_{in} to zero. At the instant that v_{s2} rises above V_{in} , the S_1 body diode starts conducting, Figure 3-16 (c), allowing S_1 to turn on at zero voltage [3-7], Figure 3-16 (d). The turn-off loss in S_2 will be low due to the presence of C_{r1} and C_{r2} and the controlled rise of v_{s2} , whilst the turn-on loss in S_1 will be virtually zero.

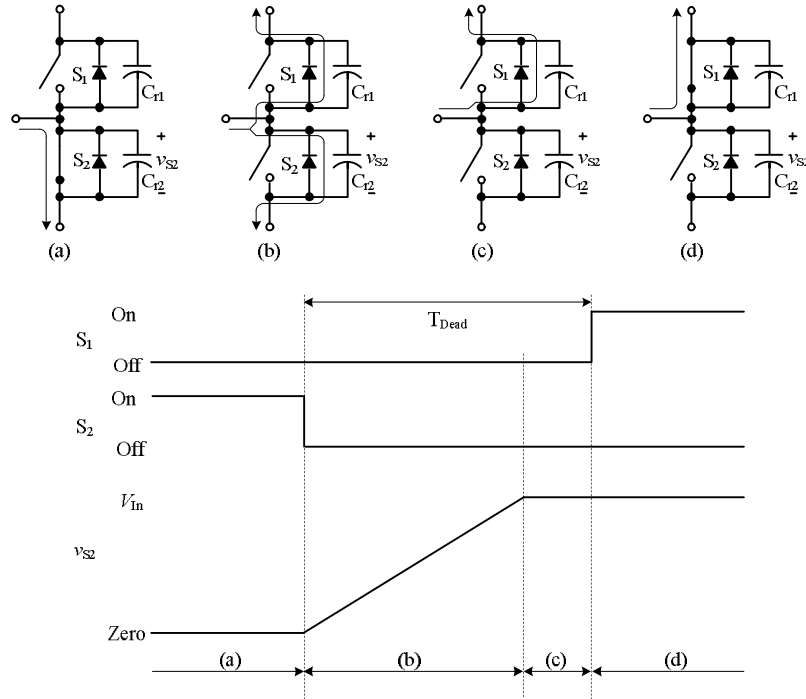


Figure 3-16 Zero-voltage commutation from S_2 to S_1 [3-7]

The negative-going transition of v_{s2} is plotted in Figure 3-17 during which i_L commutates from S_1 to S_2 . S_1 carries a positive current i_L in Figure 3-17 (a) since the inductor current is now positive. The turn-off of S_1 forces i_L to commutate from S_1 to C_{r1} and C_{r2} , Figure 3-17 (b), and the voltage on C_{r2} decreases from V_{in} to zero whilst C_{r1} charges from zero to

V_{in} . After v_{s2} reduces to zero the body diode of S_2 is forward biased and carries i_L , Figure 3-17 (c). S_2 can then be switched on under zero voltage conditions, Figure 3-17 (d). Similar to the first transition, the turn-off loss in S_1 may be limited by appropriate choice of the snubber capacitors, whilst the turn-on loss in S_2 will be virtually zero.

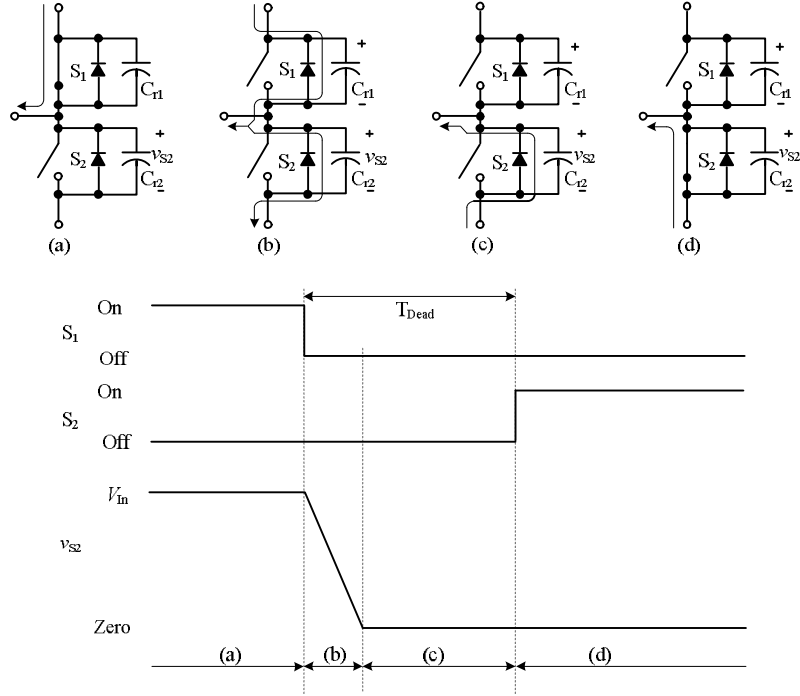


Figure 3-17 Zero-voltage commutation from S_1 to S_2

To achieve the low-loss zero-voltage-switching, the inductor current must transiently reverse. Therefore the ratio K_L in equation (3-1) must be greater than two.

$$K_L = \frac{\Delta I_L}{I_o} \quad (3-1)$$

where ΔI_L is the peak-to-peak inductor ripple current and the load current, I_o , is

$$I_o = \frac{V_o}{R} \quad (3-2)$$

ΔI_L may be calculated by (3-3) since the dead time is relatively small compared to the switching period T_s .

$$\Delta I_L = \frac{V_{in} - V_o}{L} D T_s \quad (3-3)$$

where D is the duty ratio of S_1 . Substituting (3-1) and (3-2) into (3-3) gives

$$L = \frac{1}{K_L} (1 - D) R T_s \quad (3-4)$$

provided that $V_o = D V_{in}$.

Whilst K_L must be greater than two, it is desirable to keep it as small as possible to limit the conduction losses. K_L was initially selected to be 2.4, and the required inductance was calculated to be 31.3 μH using (3-4). The precise value must be confirmed by considering the turn-off transient of S_2 ; the current must be sufficiently negative at the switching instant to ensure that the snubber capacitors are completely charged/discharged. First the snubber capacitors must be chosen by considering the S_1 turn-off transient.

Considering the S_1 turn-off transient and the residual switching loss, snubber capacitor values may be determined. The S_1 drain current may be approximated by (3-5) as the device turns off.

$$i_D = I_{L\max} \left(1 - \frac{t}{T_f}\right) \quad (3-5)$$

where $I_{L\max}$ is the maximum inductor current, assumed to remain constant during the transition, and T_f is the fall time of the drain current, calculated as 40 ns at room temperature using (2-35) in Chapter 2.

The current through the snubber capacitor C_{r1} is calculated in (3-6) assuming that $C_{r1} = C_{r1} = C_r$. The voltage across the snubber capacitor C_{r1} , which is also the drain-source voltage of S_1 , is obtained in (3-7) by integrating (3-6) and dividing by C_r .

$$i_{Cr} = \frac{I_{L\max} t}{2T_f} \quad (3-6)$$

$$v_{S1} = \frac{I_{L\max} t^2}{4C_r T_f} \quad (3-7)$$

The energy dissipated in S_1 during turn-off is obtained by integrating the product of (3-5) and (3-7) over the interval $t = 0$ to T_f , giving (3-8)

$$Q_{S1_off} = \frac{I_{L\max}^2 T_f^2}{48C_r} \quad (3-8)$$

Two 2.2 nF, 160 V polystyrene capacitors were selected for the snubbers. The drain-source capacitances of the MOSFETs are effectively in parallel with the snubbers and result in a total value for C_r across each MOSFET of 2.37 nF. With this value of capacitance the turn-off energy in S_1 , calculated from (3-8), is 4.22 μ J, resulting in an average power dissipation of 0.21 W. The turn-off energy loss in S_2 was negligibly small as the commutation current is very much lower than that in S_1 .

The duration of the voltage transitions were calculated using (3-9) to be 34 ns and 490 ns for the S_1 and S_2 turn-off transients, assuming that the inductor current is constant during the transition. The dead times were therefore set at 50 ns and 600 ns.

$$t = \frac{2C_r V_{In}}{I_{L\max/\min}} \quad (3-9)$$

3.2.3 ZVS-CV converter room temperature test

Figure 3-18 plots the drain-source voltages of the individual MOSFET devices during the two transient intervals along with the inductor current at room temperature. During the S_1 turn-off transient the inductor current is at its maximum, and the voltage transition takes about 50 ns, Figure 3-18 (a); however, it takes more than 600 ns for the voltage transition when S_2 turns off due to the small value of the inductor current at this instant, Figure 3-18 (b).

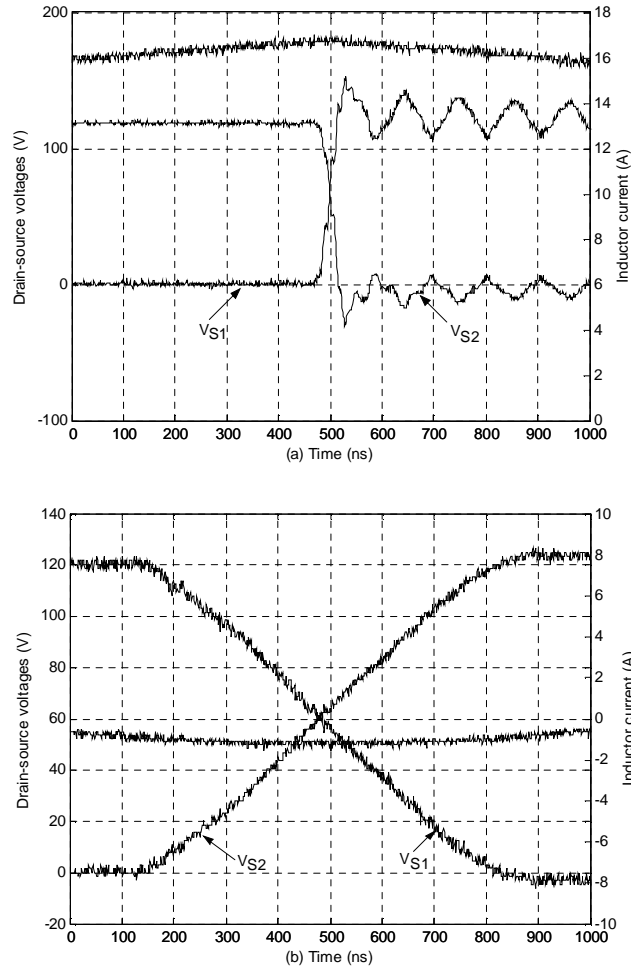


Figure 3-18 Transient waveforms: (a) S_1 turn-off transient, (b) S_2 turn-off transient in the ZVS-CV converter with two IRFB31N20D MOSFETs

$$V_{In} = 120V, V_O = 60V, P_{Load} = 480W$$

Since the inductor current flows through one or other of the MOSFETs, the total semiconductor conduction loss may be calculated from the RMS inductor current and the MOSFET $R_{DS(on)}$. The RMS value of the inductor current is obtained by (3-10) from [3-8], giving the conduction loss as 6.30 W. The total semiconductor loss was also confirmed by the measured inductor losses and the input and output powers.

$$I_{RMS} = I_o \sqrt{1 + \frac{1}{3} \left[\frac{\Delta I_L / 2}{I_o} \right]^2} \quad (3-10)$$

3.2.4 Analysis of the semiconductor losses in the 120 V ZVS-CV converter at low temperatures

The zero-voltage-switching clamped-voltage converter prototype, Figure 3-19, was bolted on top of the cold head inside the cold chamber and tested in the same manner as the previous converter prototypes.



Figure 3-19 Semiconductors and drive circuit for the 120V ZVS-CV converter

Since the snubber capacitors were soldered directly across the drain and source of the individual MOSFET devices, only the MOSFET voltage switching waveforms were

recorded by the digital oscilloscope. The measured semiconductor losses were also confirmed by measurement of the converter input and output powers using high resolution multimeters and measurement of the inductor losses.

Figure 3-20 plots the transient drain-source voltages for the individual MOSFETs at all temperatures. The waveforms on the left hand side, Figure 3-20, are the S_1 and S_2 drain-source voltages during the S_1 turn-off transient, while the transient voltages during the S_2 turn-off are on the right hand side. All voltage waveforms change very little over the temperature range 20-300 K. Therefore, the zero-voltage-switching is maintained and the switching loss is around 0.21 W determined by the S_1 turn-off loss.

Figure 3-21 plots the total semiconductor loss along with the conduction and switching losses at temperatures down to 20 K from 300 K. The total semiconductor loss decreases by more than a factor of five at low temperatures, and at 50 K it is approximately 18 % of the room temperature value.

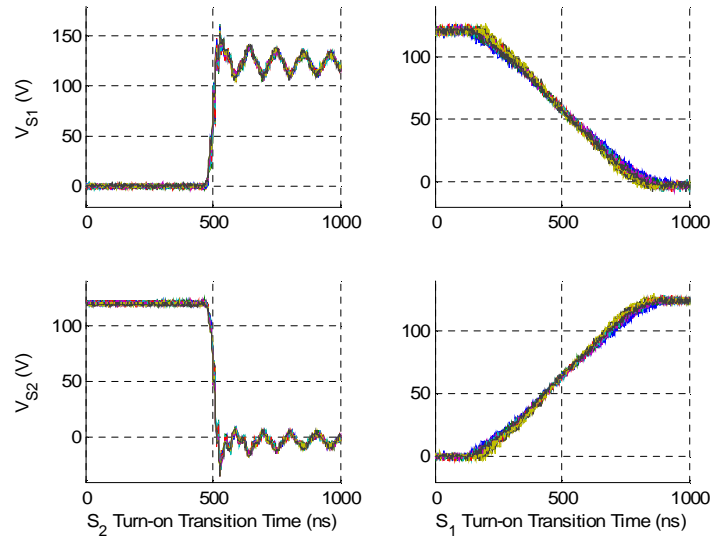


Figure 3-20 Transient voltages in the ZVS converter at a number of temperatures over the range 20-300 K with two IRFB31N20D MOSFETs,
 $V_{In} = 120V, V_O = 60V, P_{Load} = 480W$

The results confirm that the circuit works well over the entire temperature range. There is a large reduction in the semiconductor loss as the temperature falls, and since the losses are largely due to conduction, the losses could be reduced by connecting additional devices in parallel. Furthermore, the switching losses could be reduced by increasing the snubber capacitors; however this would require a larger ripple current in the inductor.

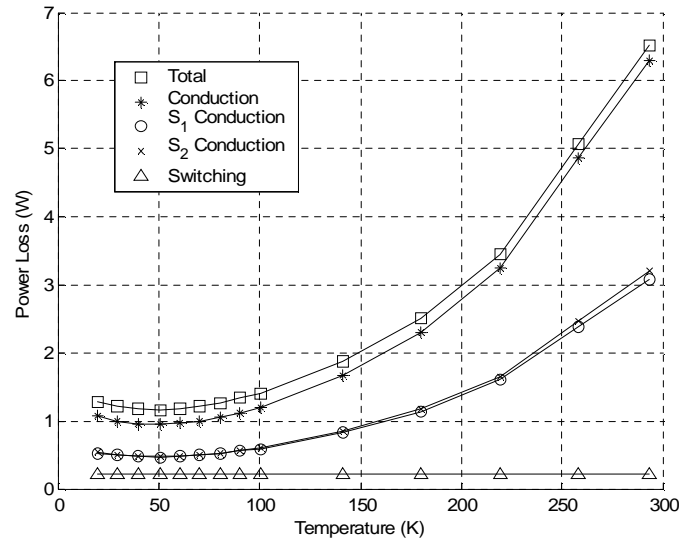


Figure 3-21 Semiconductor losses in the ZVS converter with two IRFB31N20D MOSFETs, $V_{in} = 120V$, $V_o = 60V$, $P_{Load} = 480W$

3.3 Summary of the semiconductor losses in the 120 V prototypes

Figure 3-22 plots the total semiconductor losses in the converters with 120 V input, including the three single-transistor buck converters described in Chapter 2 and the two two-transistor buck converters, whilst Figures 3-23 and 3-24 show the breakdown of the total semiconductor losses into conduction and switching losses respectively. All the 120 V prototypes are listed in Table 3-4, and the number in the three Figures is related to the prototype in Table 3-4.

Table 3-4 120 V, 480 W prototypes list

1	Hard-switching converter with an ultrafast diode
2	Hard-switching converter with a silicon Schottky diode
3	Hard-switching converter with a SiC Schottky diode
4	Synchronous rectifier
5	Zero-voltage-switching converter

Figure 3-22 shows that the soft-switched and the synchronous rectifier prototypes offer the lowest semiconductor losses. At room temperature the synchronous rectifier has a slight advantage due to its significantly lower conduction loss, Figure 3-23; the peak current levels in the soft-switching converter are much higher due to the very large inductor ripple current. However, at very low temperature the conduction losses in both prototypes reduce substantially due to the reduction in the MOSFET on-state resistance, but the switching loss remains around 1.5 W in the synchronous rectifier, Figure 3-24, whereas it is 0.21 W for the soft-switching circuit, less than one-seventh of the value in the synchronous rectifier. Therefore, at cryogenic temperatures the soft-switching prototype has superior performance.

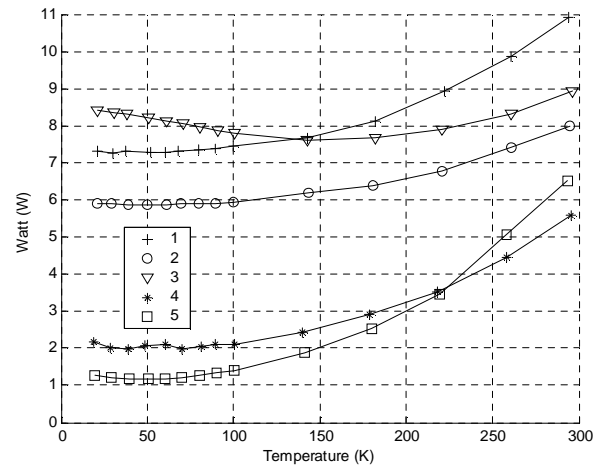


Figure 3-22 Semiconductor losses in the 120 V prototypes

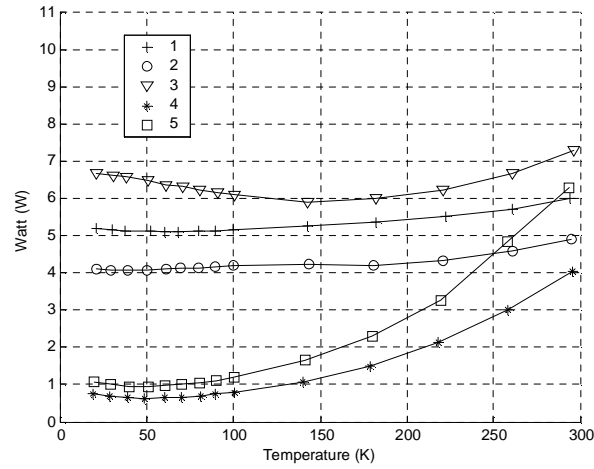


Figure 3-23 Conduction losses in the 120 V prototypes

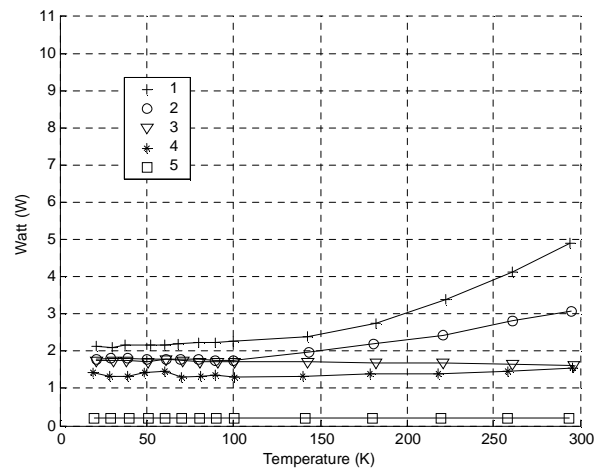


Figure 3-24 Switching losses in the 120 V prototypes

3.4 Conclusions

- The synchronous rectifier has the capability of operating from high voltage levels, 120 V and 500 V. And the peak reverse current through the S_2 body diode was less than half the value measured with a dead time of 50 ns in the 120 V synchronous rectifier, using the optimised dead time control. However, the increase in the threshold voltage at low temperature required the dead time to be reduced at cryogenic temperatures.
- The temperature invariant switching losses limited the performance of the synchronous rectifier circuit at cryogenic temperatures whereas the much lower switching losses in the zero-voltage-switching circuit allowed the overall losses to fall almost in proportion with the reduction in the MOSFET on-state resistance. The total semiconductor loss at 50 K in the zero-voltage-switching circuit was 18 % of the room temperature value and the losses could easily be reduced further by adding additional MOSFETs in parallel.
- An additional advantage of the synchronous rectifier over the diode based circuits is that the semiconductor conduction losses will be largely independent of duty ratio for a specific output current.

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Chapter 4

Cryogenic operation of three-level diode-clamped step-down converters

This Chapter describes the performance of the multi-level step-down converter at low temperatures. A three-level, diode-clamped, DC-DC step-down converter is chosen for design and prototyping to operate from 500 V and 600 V DC supplies. Power MOSFETs are employed in the prototypes with ultrafast and silicon carbide diodes. The semiconductor losses are evaluated in the temperature range 20-300 K. Finally a zero-voltage-switching version of the multi-level converter is proposed to overcome the switching loss limitations of the circuit.

4.1 Three-level converter design and operation

One possible application for power electronics in a cryogenic environment is for the control of the DC current in a superconducting coil, for example the field coil in a superconducting synchronous machine, or the coil of a superconducting magnet energy storage device (SMES). The DC supply in these examples could be at quite a high voltage, implying the use of high voltage MOSFETs or IGBTs in the step-down DC-DC converter [4-1, 4-2, 4-3]. To enable the use of lower voltage MOSFETs, which have the attraction of lower on-state resistance and therefore lower losses, a multi-level circuit is considered [4-4, 4-5, 4-6]. In general, an n -level step-down converter imposes a maximum off-state voltage across the

devices of $V_{in}/(n-1)$, where V_{in} is the DC supply voltage. Multi-level circuits overcome the voltage sharing problems of simply connecting devices in series.

4.1.1 Three-level, diode-clamped, step-down converter design

A three-level, diode-clamped converter is shown in Figure 4-1. Two transistors are connected in series in each leg, S_{T1} and S_{T3} in leg a, S_{T2} and S_{T4} in leg b. Two series connected capacitors, C_{in1} and C_{in2} , are used to divide the supply voltage into two equal levels of $V_{in}/2$, and the clamping diodes, D_{C1} and D_{C2} , limit the maximum voltage across each transistor to $V_{in}/2$.

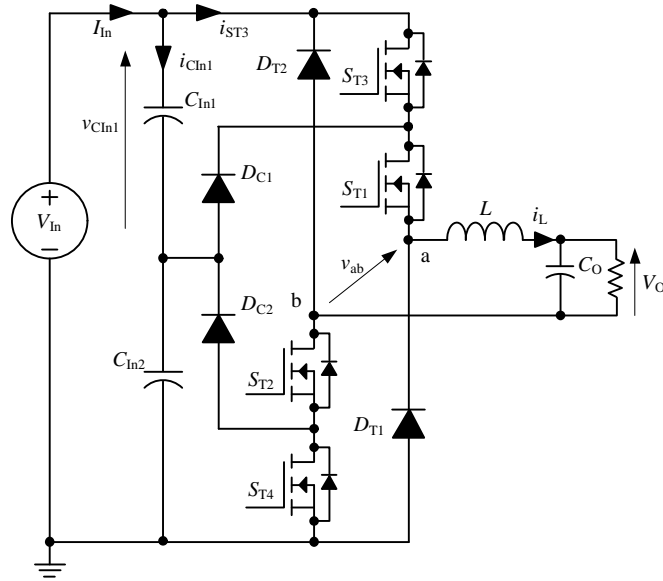


Figure 4-1 Three-level, diode-clamped DC-DC converter

The complete set of sub-topologies of the three-level converter is displayed in Figure 4-2, assuming continuous conduction of the current in the filter inductor L . It is seen that different sub-topologies produce different voltages across the output, v_{ab} , Figure 4-1. By appropriate choice of the sub-topologies and the durations of the sub-topologies, the local average of v_{ab} can be controlled to any desired value in the range $-V_{in} < v_{ab} < V_{in}$. For a unidirectional inductor current i_L , the direction of power flow depends on the polarity of the average v_{ab} .

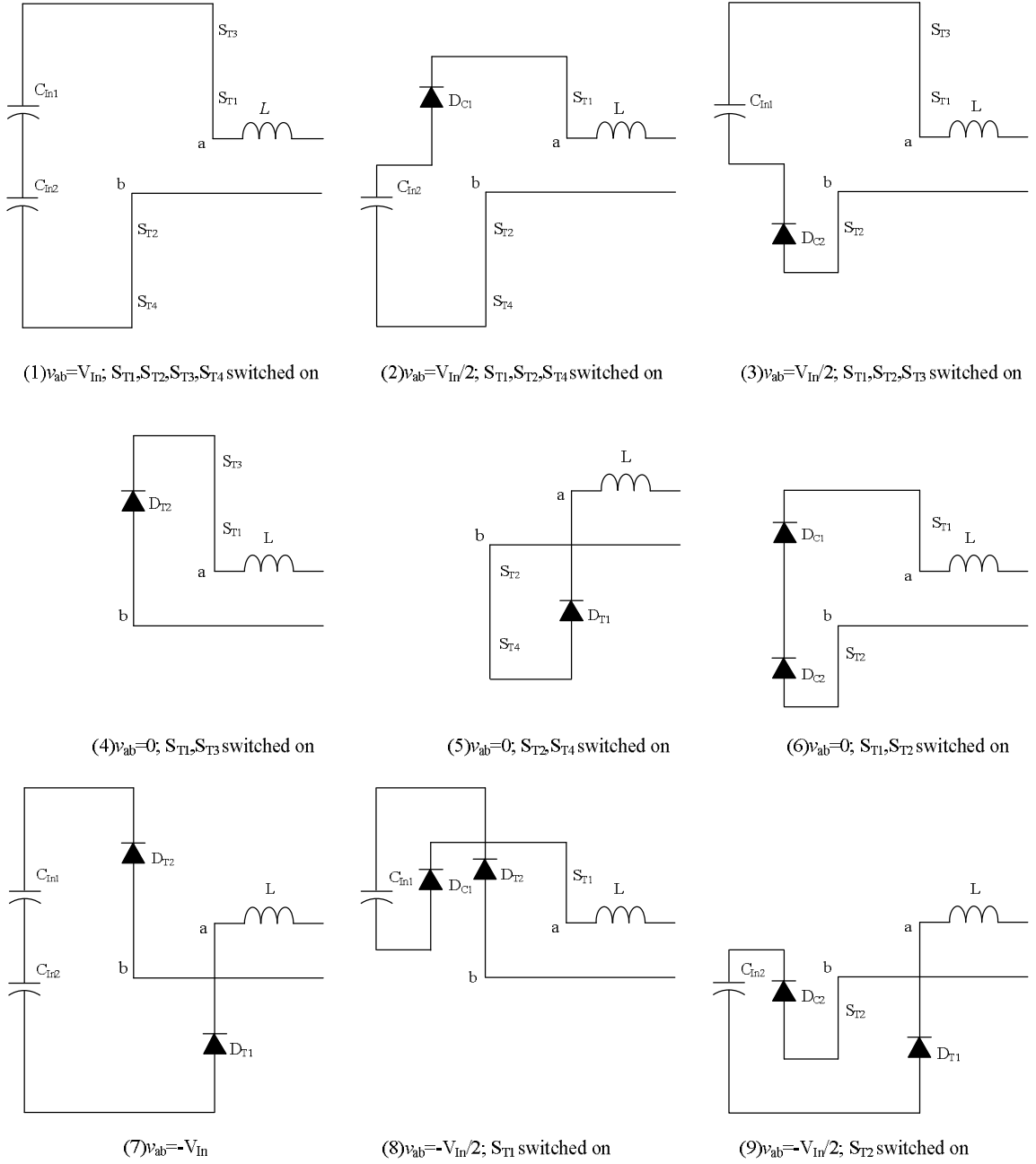


Figure 4-2 Sub-topologies of the three-level converter [4-4]

Figure 4-2 shows that more than one sub-topology is available to achieve $v_{ab} = -V_{in} / 2$, 0 and $V_{in} / 2$, therefore through careful use of the redundant states, PWM schemes can be developed to reduce switching losses and output current ripple, and also to maintain the charge balance of the two series connected capacitors [4-4]. The basic principle is to operate

the converter only with the sub-topologies which produce output voltage levels directly adjacent to the required V_o at any given time. This results in reduced switching losses and filter inductor current ripple [4-4]. The active sub-topologies and switch control strategies for different ranges of V_o are listed in Table 4-1, in which the sub-topology numbers refer to those in Figure 4-2. In each of the operating ranges listed in Table 4-1, the pair of devices that are switched are operated in an interleaved manner; the devices being switched on in alternate half cycles for a time DT_s , where D is the duty ratio and T_s is the period.

Table 4-1 Three-level two-quadrant control strategy [4-4]

Operating Range	Active Subtopologies	PWM Strategies
$-1 < V_o/V_{In} < -0.5$	(7), (8), (9)	S_{T1}, S_{T2} : PWM control S_{T3}, S_{T4} : Always Off
$-0.5 < V_o/V_{In} < 0$	(6), (8), (9)	S_{T1}, S_{T2} : PWM control S_{T3}, S_{T4} : Always Off
$0 < V_o/V_{In} < 0.5$	(2), (3), (6)	S_{T1}, S_{T2} : Always On S_{T3}, S_{T4} : PWM control
$0.5 < V_o/V_{In} < 1$	(1), (2), (3)	S_{T1}, S_{T2} : Always On S_{T3}, S_{T4} : PWM control

The principal waveforms are shown in Figure 4-3 for the operation with 75 % duty ratio. Since S_{T1} and S_{T2} , are permanently on their control signals are not plotted. When S_{T3} is switched on, S_{T4} is already on and the circuit configures into sub-topology (1), Figure 4-2. Current flows through S_{T1} , S_{T2} , S_{T3} , S_{T4} and the output filter, increasing the output inductor current. When S_{T4} turns off, S_{T3} is still on and the circuit is switched into sub-topology (3), Figure 4-2, where the inductor current freewheels through S_{T1} , S_{T2} , S_{T3} and the diode D_{C2} . The subsequent turn-on of S_{T4} at the start of the next half-cycle then changes the circuit again into sub-topology (1), Figure 4-2, which increases the inductor current. When S_{T3} turns off, S_{T4} continues to conduct and the circuit is switched into sub-topology (2), Figure 4-2, the inductor current freewheels through S_{T1} , S_{T2} , S_{T4} and the diode D_{C1} until S_{T3} turns on and the cycle repeats. The off-state voltages across S_{T3} and S_{T4} are $V_{In}/2$ and the frequency of the inductor ripple current is twice the switching frequency, Figure 4-3.

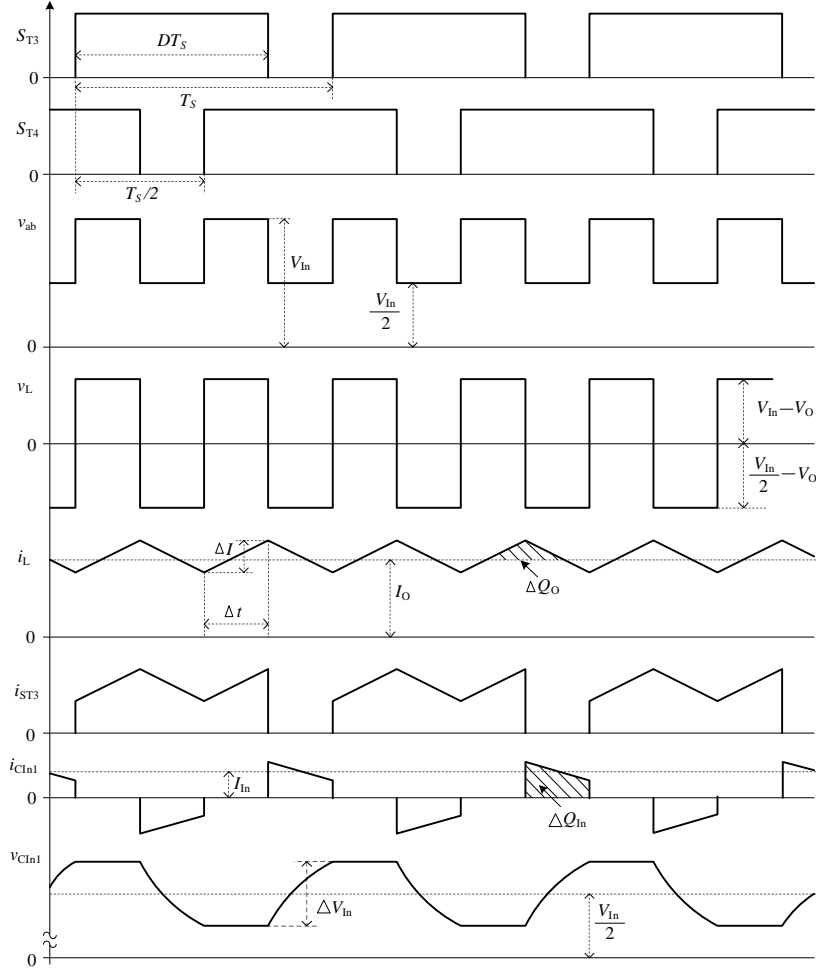


Figure 4-3 Main waveforms at 75% duty ratio

By examining the v_{ab} waveform, the average converter output voltage may be calculated as:

$$V_o = \frac{[V_{in}(T_s/2 - (1-D)T_s) + V_{in}/2(1-D)T_s]}{T_s/2} = DV_{in} \quad (4-1)$$

By similar consideration of the waveforms at transistor duty ratios below 0.5, the voltage conversion ratio may again be given by the expression in equation (4-1).

Considering the inductor volt-second balance, the peak-to-peak inductor current ripple may be calculated by equation (4-2).

$$\Delta I_L = \frac{v_L \Delta t}{L} \quad (4-2)$$

where Δt is defined in Figure 4-3. Substituting $\Delta t = DT_s - T_s / 2$ and rearranging (4-2), the output inductor value may be calculated using (4-3).

$$L = \frac{(V_{in} - V_o)(2D - 1)T_s}{2\Delta I_L} \quad (4-3)$$

Assuming the inductor ripple current flows entirely in the output capacitor the peak-to-peak output voltage ripple may be expressed in (4-4)

$$\Delta V_o = \frac{\Delta Q_o}{C_o} = \frac{1}{C_o} \times \frac{1}{2} \frac{\Delta I_L}{2} \frac{T_s}{4} \quad (4-4)$$

where ΔQ_o is the charge flow to/from the capacitor each half cycle, Figure 4-3. Rearranging (4-4) and substituting for ΔI_L from (4-3), the output capacitance is obtained in (4-5).

$$C_o = \frac{(V_{in} - V_o)(2D - 1)T_s^2}{32L\Delta V_o} \quad (4-5)$$

Considering a constant source current I_{in} , Figure 4-1, the input capacitor, C_{in1} , is charged during the off-time of S_{T3} , and discharged when S_{T4} is off, Figure 4-3. The capacitance may be calculated using (4-6)

$$C_{in} = \frac{\Delta Q_{in}}{\Delta V_{in}} = \frac{I_{in}(1 - D)T_s}{\Delta V_{in}} \quad (4-6)$$

where ΔQ_{in} is the charge flow to/from the capacitor each half cycle, Figure 4-3.

To allow the operation of the converter to be examined at two input voltage levels and duty ratios, prototypes were designed to operate with $D = 0.5$ from a 500 V supply and with $D = 0.75$ from a 600 V supply, all transistors switching at 50 kHz. The 500 V results will then be compared with those from the 500 V prototypes described in Chapters 2 and 3.

The detailed design requirements of the two three-level, buck converters are listed in Table 4-2. Applying the design requirements to the equations (4-3), (4-5) and (4-6), the values of the input capacitor, filter inductor and capacitor are calculated and listed in Table 4-3.

Table 4-2 Three-level buck converter design requirements

Input Voltage (V)	500	600
Input Current (A)	1	1
Input Power (W)	500	600
Output Voltage (V)	250	450
Output Current (A)	2	1.33
Duty Ratio	0.5	0.75
Frequency (kHz)	50	50
Input Voltage Ripple (V)	25	30
Output Voltage Ripple (V)	2.5	4.5
Inductor Current Ripple (A)	0.3	0.2

Table 4-3 Three-level converter passive component design values

Circuit	Input Capacitor (C_{In1}, C_{In2})	Filter Inductor (L)	Filter Capacitor (C_o)
500 V	800 nF	4.17 mH	150 nF
600 V	333 nF	3.75 mH	56 nF

4.1.2 Three-level, diode-clamped, step-down converter fabrication

Two 400 V, 2.2 μ F polyester capacitors were chosen as the input capacitors, C_{In1} and C_{In2} . Four power MOSFETs, IRFIB7N50A ($V_{BR} = 500V, R_{DS(on)} = 0.52\Omega @ 25^\circ C$), were used as the switching transistors. Two silicon carbide Schottky barrier diodes, CSD10120 ($V_{BR} = 1200V, V_F = 1.6V$ at 10 A and $25^\circ C$), were employed as the bridge diodes, D_{T1} and D_{T2} . Two ultrafast diodes, MUR1560 ($V_{BR} = 600V, V_F = 1.5V$ at 15 A and $25^\circ C$), were used

as the voltage-clamping diodes, D_{C1} and D_{C2} . Totally, there were ten components in the conversion circuit, which were all mounted on a round copper plate with 120 mm diameter and connected by a PCB board. A second pair of prototypes was built by replacing the ultrafast voltage-clamping diodes with the silicon carbide Schottky diodes, CSD06060 ($V_{BR} = 600V, V_F = 1.6V$ at 6 A and 25°C). A UC3524 PWM integrated circuit was used to generate the driving signals for the MOSFETs S_{T3} and S_{T4} . The MOSFETs S_{T1} and S_{T2} , were held permanently on using floating 12 V supplies.

4.2 Single device characteristic at low temperatures

To enable the device losses to be determined in the converters, the on-state resistances and voltages of the devices were measured at the converter operating current levels using the methods described previously.

4.2.1 MOSFET on-state resistance at low temperatures

The power MOSFET IRFIB7N50A on-state resistance was measured over the temperature range 20-300 K at the currents of 2 A and 1.33 A, using the test configurations described in Chapter 2, Section 2.4.1.

Figure 4-4 plots the on-state resistances across the temperature range at two current levels. There is no significant difference between the resistances at 1.33 A and 2 A. The on-state resistance has a minimum value of 52 mΩ at 70 K, one eighth of the room temperature value. The proportionate decrease in on-state resistance is much greater than that measured for the CoolMOS SPP20N60C3 device, Figure 2-11, which was assumed to be due to the conventional structure of the IRFIB7N50A.

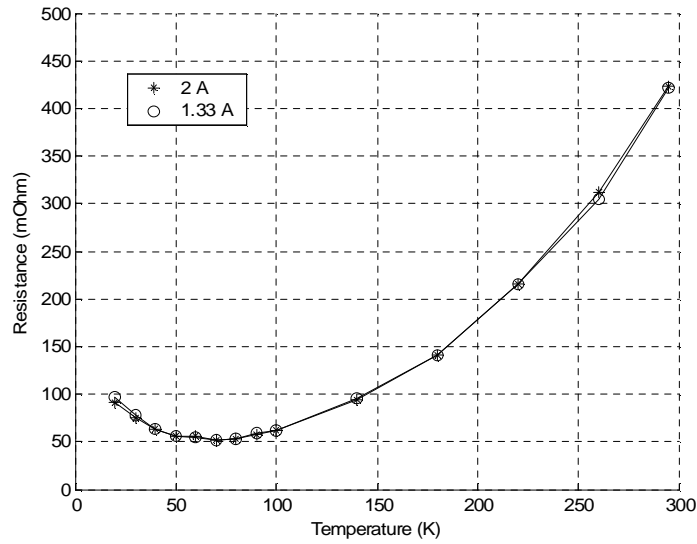


Figure 4-4 Measured on-state resistance for the IRFIB7N50A

4.2.2 Diode on-state voltage at low temperatures

The on-state voltages of the ultrafast diode MUR1560 and the silicon carbide Schottky barrier diode CSD06060 were examined across the range 20-300 K at the forward currents of 2 A and 1.33 A, using the method in Chapter 2, Section 2.4.2. Both on-state voltages, Figure 4-5, show the same temperature dependencies as described in Chapter 2, Section 2.4.2 over the temperature range, and the on-state voltage increases with the increase in forward current. However, the on-state voltage of the CSD06060 diode is slightly higher than that of the CSD10060.

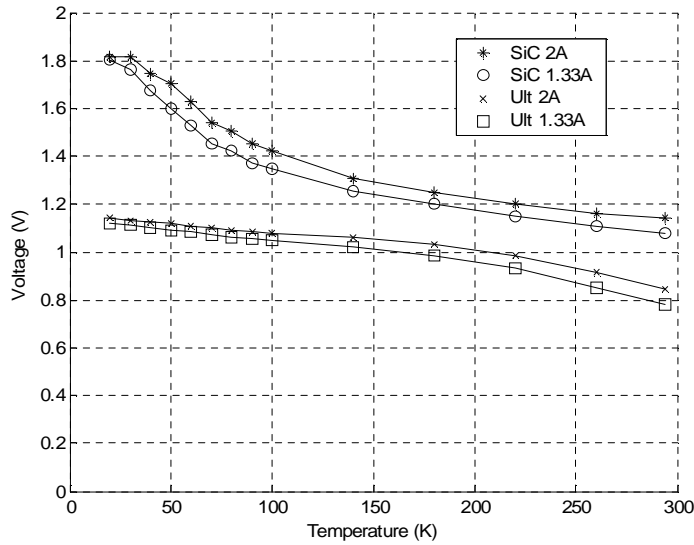


Figure 4-5 Measured on-state voltages for the CSD06060 and MUR1560

4.2.3 Capacitor characteristics at low temperatures

The 400 V, 2.2 μF polyester capacitor was tested at low temperatures. The capacitance and the series resistance were measured using the Agilent 4284A precision LCR meter at temperatures down to 20 K. Figure 4-6 plots the capacitance at 50 kHz and 100 kHz over the temperature range 20-300 K, while Figure 4-7 shows the dissipation factor. The capacitance is insensitive to temperature, decreasing by 5.6 % at 20 K compared to room temperature. There is no significant difference between the capacitances at the two frequencies. The dissipation factor decreases with a decrease in temperature due to the reduction in the equivalent series resistance. These results are consistent with those reported in the literature for similar capacitor types [4-7, 4-8]. The RMS current through the input capacitor is to be 0.5 A based on the waveforms, Figure 4-3. The power loss in each capacitor is calculated to be 3.75 mW due to the equivalent series resistance at room temperature, which will decrease with a decrease in temperature. Therefore the power loss in the input capacitors is very small and can be omitted at all temperatures.

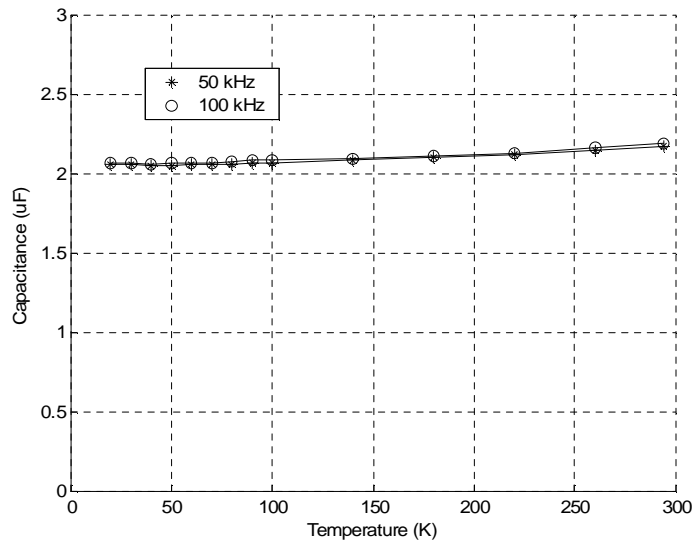


Figure 4-6 Measured capacitance for the 400 V, 2.2 μ F polyester capacitor

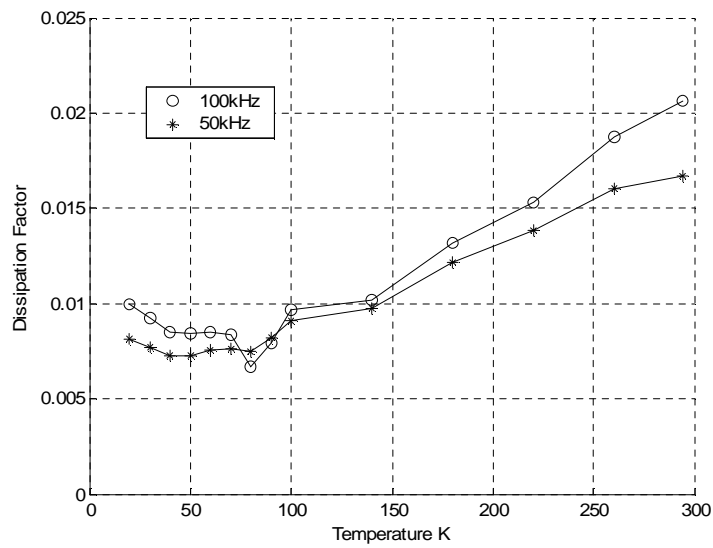


Figure 4-7 Measured dissipation factor for the 400 V, 2.2 μ F polyester capacitor

4.3 Analysis of the semiconductor losses in the three-level converters at low temperatures

Figure 4-8 shows the three-level, diode-clamped, step-down converter prototype. The capacitors C_{in1} and C_{in2} were clamped to the copper base plate to ensure that they operate at low temperature. Figure 4-9 displays the cryogenic test layout. The prototype was mounted on the cold head in the vacuum chamber, the input and output filters were on the left hand side outside the chamber, and the PWM control signals conveyed by the signal feedthrough were on the right hand side. An 8-pin power feedthrough, Figure 4-10, was used to connect the circuit points labelled in Figure 4-10 (b) to the outside of the vacuum chamber. Therefore, the circuit connection between the voltage-clamping diodes and the mid-point of the input capacitors was made outside the cold chamber. This was necessary in order to monitor the currents in the voltage-clamping diodes, but has the disadvantage of introducing stray inductance into the circuit connections. The wires were practically cut as short as possible and twisted to minimise the stray inductance.

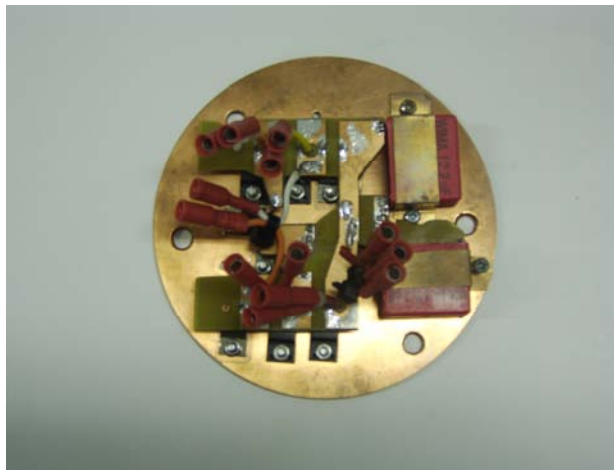


Figure 4-8 Three-level, diode-clamped, step-down converter prototype

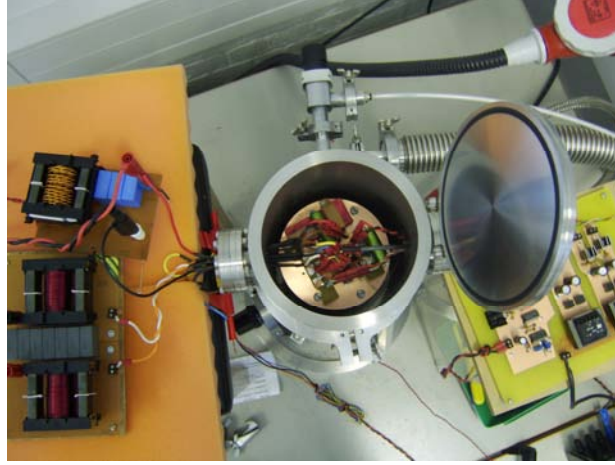


Figure 4-9 Three-level prototype cryogenic test layout

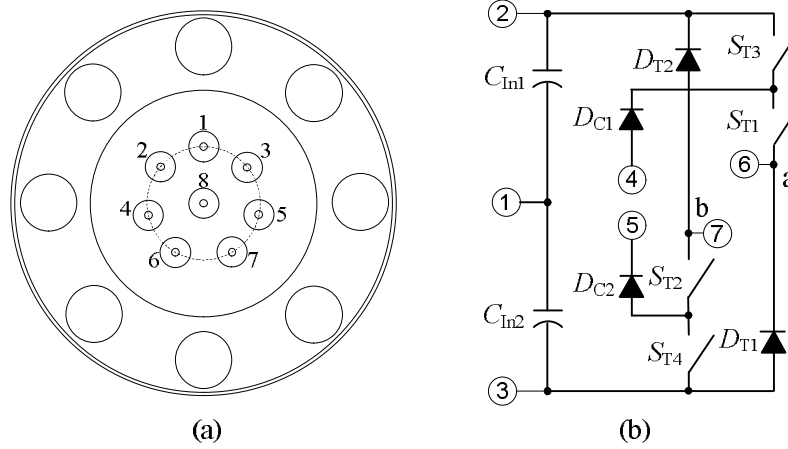


Figure 4-10 Schematic connection for the power feedthrough

The converter operation was examined at a set of temperature points over the range of 20-300 K and the switching losses were obtained by the switching frequency multiplied by the time integral of the device voltage and current product, whilst the on-state losses were calculated by equations (4-7), (4-8) and (4-9) from a knowledge of the current level and the device characteristics in Figures 4-4 and 4-5. The measured semiconductor losses were confirmed by measurement of the converter input and output powers using high resolution multimeters and measurement of the inductor losses.

$$P_{Cond_ST1\&ST2} = 2 \times I_{RMS}^2 \times R_{DS(on)} \quad (4-7)$$

$$P_{Cond_ST3\&ST4} = 2 \times I_{RMS}^2 \times R_{DS(on)} \times D \quad (4-8)$$

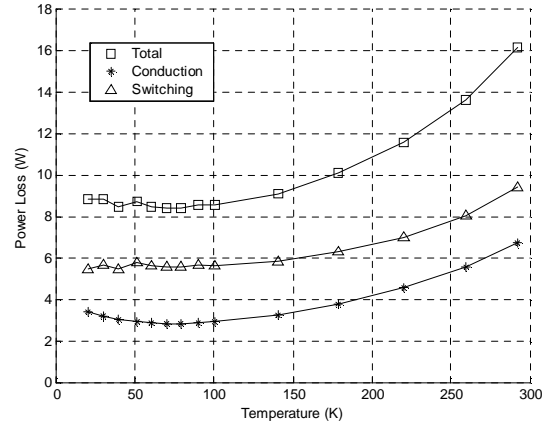
$$P_{Cond_DC1\&DC2} = 2 \times I_{AV} \times V_F \times (1 - D) \quad (4-9)$$

4.3.1 Ultrafast diode based, three-level, buck converter (500 V supply)

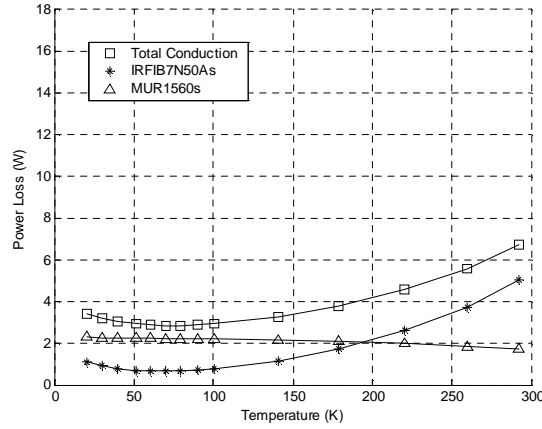
To operate with a duty ratio of 0.5, sub-topologies (1) and (6), Figure 4-2, were used and the MOSFETs S_{T3} and S_{T4} were switched in synchronism.

The ultrafast diode MUR1560 based, three-level prototype was tested at low temperatures operating from a 500 V supply. Figure 4-11 (a) plots the total semiconductor losses in the temperature range 20-300 K, along with the conduction and switching losses. Figures 4-11 (b) and (c) display the losses in the individual semiconductors.

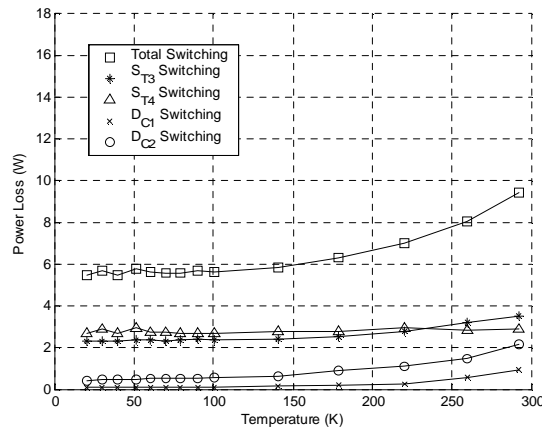
The total semiconductor loss decreases nearly by a half at 100 K, Figure 4-11 (a), due to the 40 % reduction in the switching loss and 60 % decrease in the conduction loss; below 100 K the total loss is insensitive to temperature, since both the switching and conduction losses change little. Figure 4-11 (b) shows that the MOSFET conduction losses decrease significantly, offset by the increase in the diode conduction losses. The switching losses in the MOSFETs dominate the total switching loss, Figure 4-11 (c), especially at low temperature. The switching loss in S_{T3} , D_{C1} and D_{C2} decreases almost by a half across the range, whereas the S_{T4} switching loss decreases slightly.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 4-11 Semiconductor losses in the three-level converter with IRFIB7N50A MOSFETs and MUR1560 diodes, $V_{In} = 500V$, $V_O = 250V$, $P_{Load} = 500W$

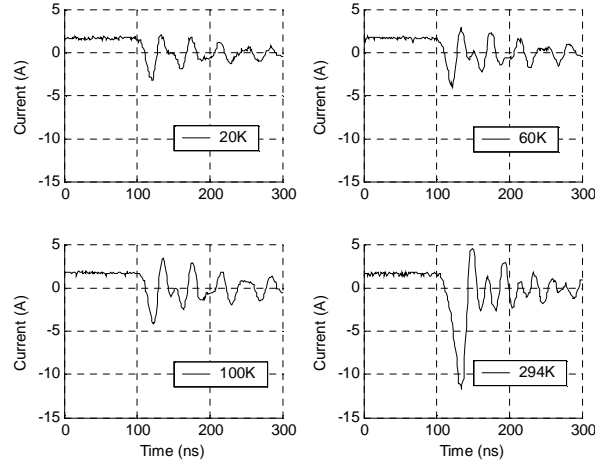


Figure 4-12 D_{C1} (MUR1560) diode turn-off currents in the three-level converter

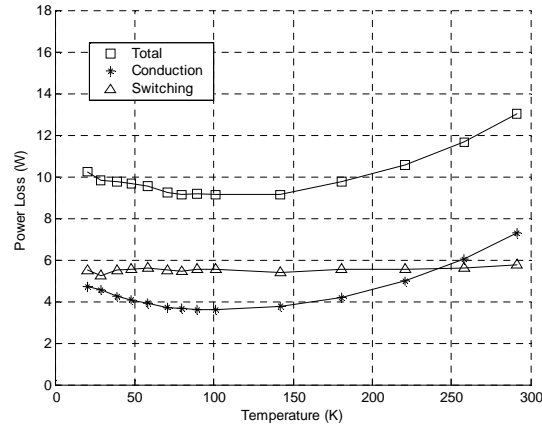
$$V_{In} = 500V, V_O = 250V, P_{Load} = 500W$$

The reduction in the switching loss at low temperature, Figure 4-11, was attributed to the improvement in the ultrafast diode reverse recovery as described in Chapter 2. Figure 4-12 plots the turn-off currents of D_{C1} at 20 K, 60 K, 100 K and 294 K. The peak reverse recovery current decreases by two-thirds and the reverse recovery time decreases by a half at 100 K, below 100 K the decrease becomes relatively small.

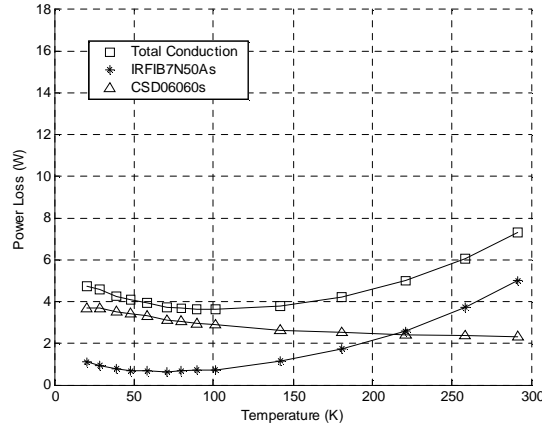
4.3.2 SiC diode based, three-level, buck converter (500 V supply)

The silicon carbide diode CSD06060 based, three-level, prototype was tested at low temperatures operating from 500 V. Figure 4-13 (a) plots the total semiconductor losses, the conduction and switching losses in the temperature range 20-300 K. The losses in the individual semiconductors are displayed in Figures 4-13 (b) and (c).

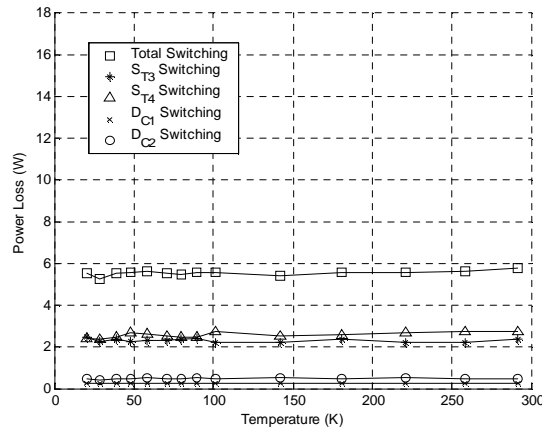
The total semiconductor loss decreases by 30 % at 80 K compared to 300 K, Figure 4-13 (a), essentially due to the 50 % reduction in the conduction loss, although the decrease in the MOSFET conduction losses is offset by the increase in the diode conduction losses, Figure 4-13 (b). All switching losses change little with temperature, Figure 4-13 (c), attributed to the temperature-invariant SiC diode switching property as observed in Chapter 2.



(a) Total semiconductor losses



(b) Conduction losses



(c) Switching losses

Figure 4-13 Semiconductor losses in the three-level converter with IRFIB7N50A MOSFETs and CSD06060 diodes, $V_{in} = 500V$, $V_O = 250V$, $P_{Load} = 500W$

4.3.3 Summary of the semiconductor losses in the 500 V prototypes

The 500 V, 500W prototypes that have been examined in this Thesis at low temperatures are listed in Table 4-4.

Table 4-4 500 V, 500 W prototypes list

1	Ultrafast diode based single-transistor step-down converter, Section 2.6.1
2	SiC diode based single-transistor step-down converter, Section 2.6.2
3	Synchronous rectifier, Section 3.1.4.2
4	Ultrafast diode based three-level step-down converter, Section 4.3.1
5	SiC diode based three-level step-down converter, Section 4.3.2

The total semiconductor losses in the five converters are plotted in Figure 4-14 in the temperature range 20-300 K, whilst Figures 4-15 and 4-16 display the breakdown of the total semiconductor losses into conduction and switching losses respectively. The numbering of the curves in the Figures follows the list in Table 4-4.

Comparing the results in Figure 4-14, the losses in the multi-level circuit are the highest at room temperature and are just below that of the synchronous rectifier at low temperature. All the circuits show fairly high semiconductor losses and the losses do not exhibit such a large reduction at low temperatures as was seen for the lower voltage circuits, Figure 3-22. This is due to a combination of factors, but mainly the lower current levels in the circuits, the large number of devices in the multi-level circuits, especially diodes, and the high switching losses in all circuits.

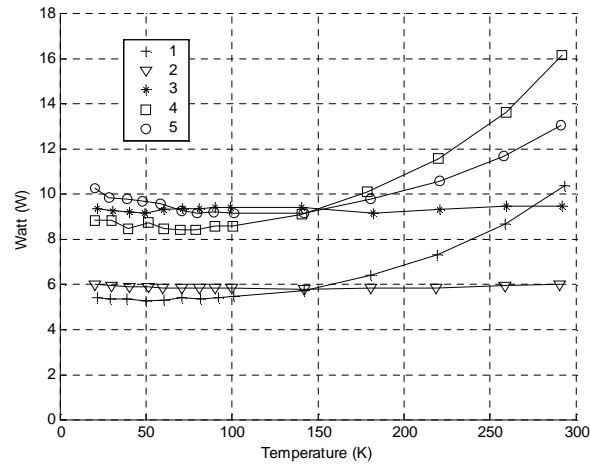


Figure 4-14 Total semiconductor losses in the 500 V prototypes

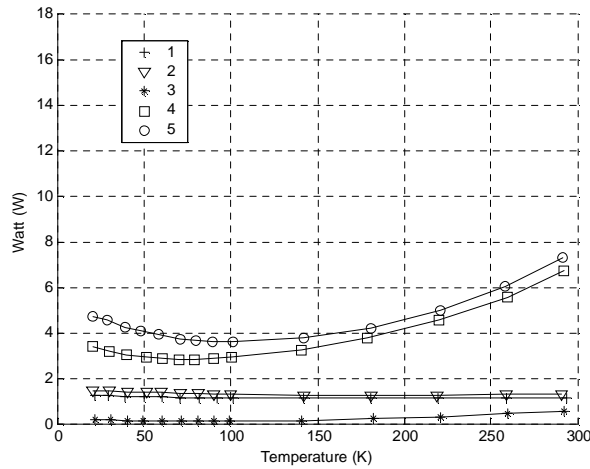


Figure 4-15 Conduction losses in the 500 V prototypes

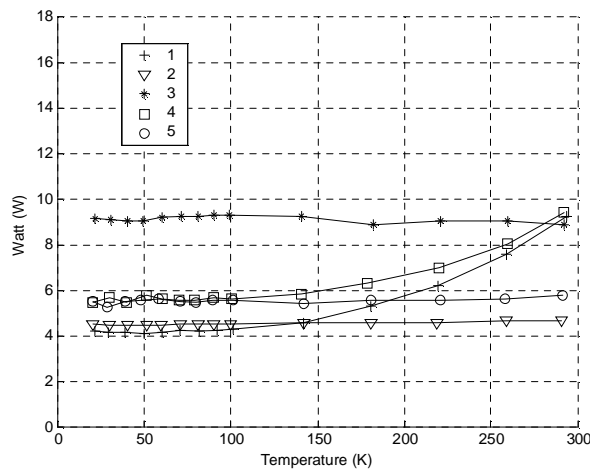


Figure 4-16 Switching losses in the 500 V prototypes

4.3.4 Three-level buck converter cryogenic operations (600 V supply)

To operate with a duty ratio of 0.75, sub-topologies (1), (2) and (3), Figure 4-2, were used and the MOSFETs S_{T3} and S_{T4} were switched at 50 kHz as shown in Figure 4-3.

The ultrafast diode and SiC diode based three-level, step-down converters were tested at low temperatures, operating from a 600 V supply and delivering 600 W to a 450 V resistive load. The total semiconductor losses for both converters are plotted in Figure 4-17, while the breakdown of the total semiconductor losses into the conduction and switching losses are plotted in Figures 4-18 and 4-19 respectively.

Compared with the results from the multi-level circuits at 500 V, Figures 4-14 to 4-16, the data in Figures 4-17 to 4-19 show very similar trends; however, the total losses are lower due to the lower current in the devices and the reduced conduction times for the voltage-clamping diodes.

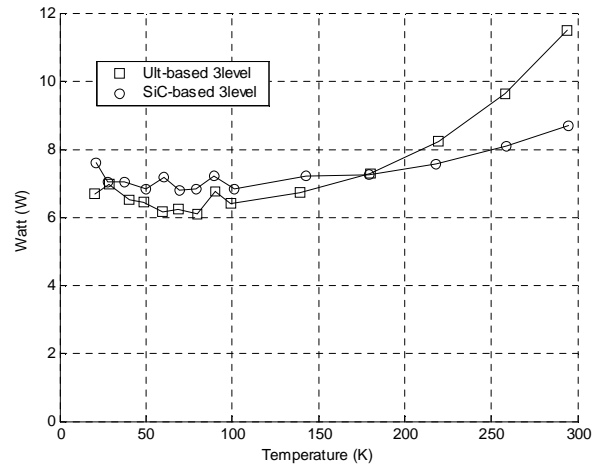


Figure 4-17 Total semiconductor losses in the 600 V prototypes

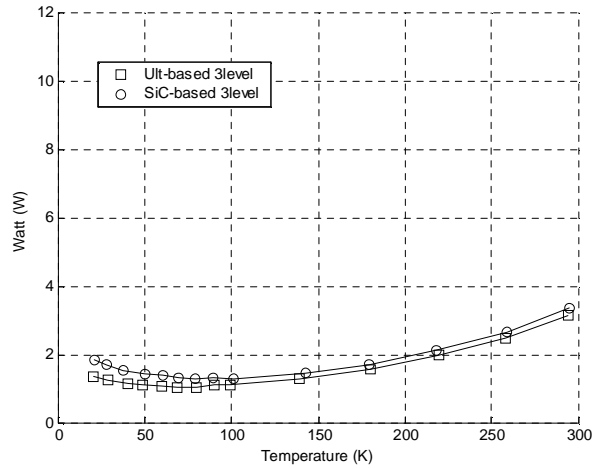


Figure 4-18 Conduction losses in the 600 V prototypes

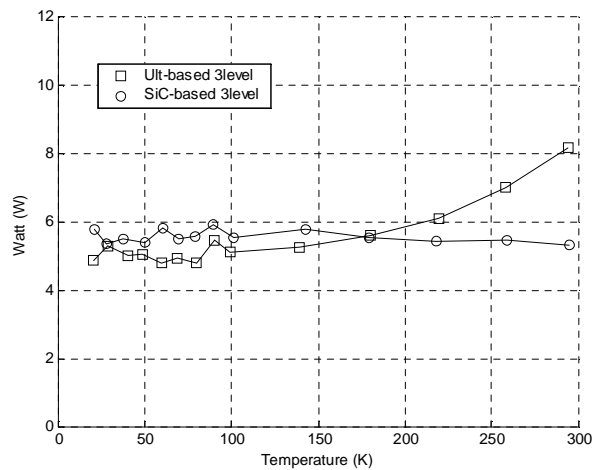


Figure 4-19 Switching losses in the 600 V prototypes

4.4 Three-level, zero-voltage-switching, step-down converter

Evaluation of the semiconductor losses in the three-level, step-down converters shows that the total semiconductor loss, conduction loss and switching loss are higher than in the corresponding single-transistor step-down converters, although they are more sensitive to temperature, Figure 4-14. The increase in losses is essentially due to the increased number of devices.

The conduction losses in the three-level circuit could be reduced at low temperature by using a synchronous rectifier for the voltage-clamping diodes. Furthermore the switching losses could be virtually eliminated by using zero-voltage-switching techniques, as discussed in Chapter 3. Therefore, a novel three-level, ZVS, step-down converter is introduced in Figure 4-20, where the voltage-clamping diodes, D_{C1} and D_{C2} , are replaced by the MOSFETs, S_{C1} and S_{C2} . A snubber capacitor is connected across the drain and source of each MOSFET. The output inductor has a bi-directional current due to the reduced inductor value and the inductor current charges/discharges the snubber capacitors in a lossless manner at each MOSFET turn-off instant. The individual MOSFETs are triggered on only after the corresponding body diode is forward conducting, achieving zero-voltage-switching.

Considering the converter operation at 25 % duty ratio as an example, the two MOSFETs, S_{T1} and S_{T2} , are permanently on, while the MOSFETs, S_{T3} and S_{T4} , are switched on in alternate half cycles with 25 % duty ratio. The MOSFETs, S_{C1} and S_{C2} , are triggered in anti-phase with S_{T3} and S_{T4} respectively, a dead time being inserted to allow charging /discharging of the snubber capacitors. The ideal waveforms are shown in Figure 4-21, where the control signals for S_{T1} and S_{T2} are omitted since they are permanently on, the other MOSFET control signals, the voltages across the snubber capacitors and the inductor current are plotted. The waveforms are defined in the circuit diagram of Figure 4-20.

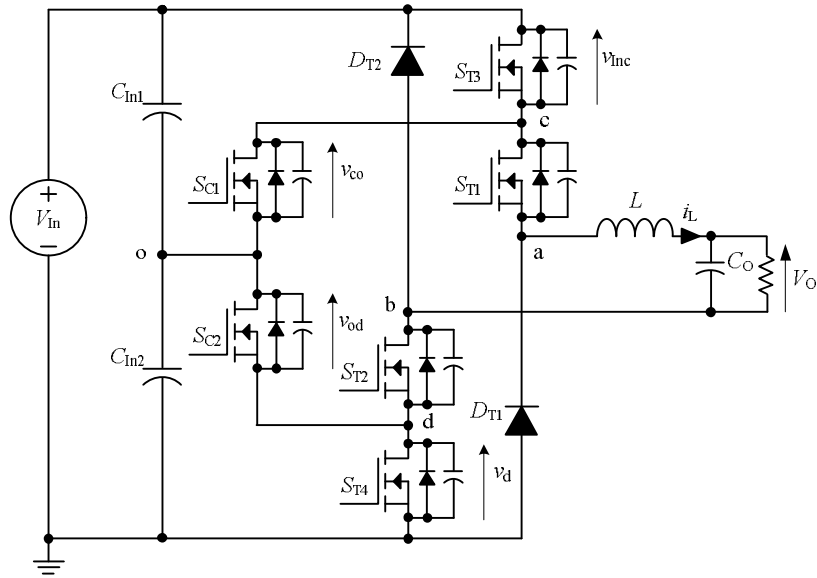


Figure 4-20 Three-level, ZVS, step-down converter

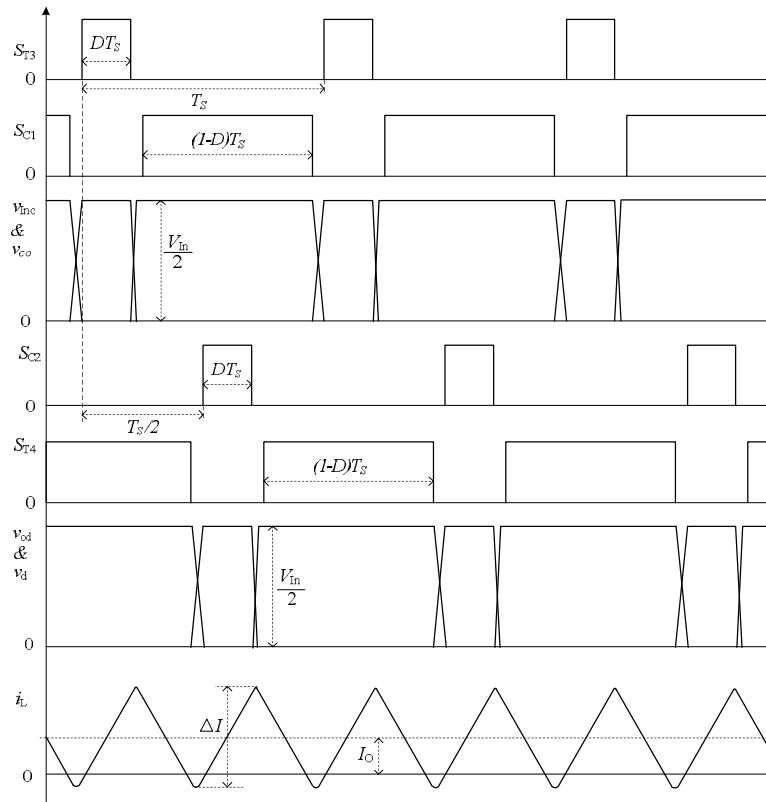


Figure 4-21 Ideal waveforms for the three-level ZVS converter, $D = 0.25$

The sub-topologies that the converter is switched through are plotted in Figure 4-22 for the three-level, ZVS converter with the power transfer from V_{in} to V_o . In sub-topology (a), Figure 4-22, S_{T3} and S_{T4} are off whilst S_{C1} , S_{C2} , S_{T1} and S_{T2} are on. The inductor current freewheels through S_{T1} , S_{T2} , S_{C1} , and S_{C2} , falling and eventually reversing. The zero-voltage-switching transient that occurs when S_{C1} turns off is shown in Figure 4-23. The inductor current charges/discharges the snubber capacitors across S_{C1} and S_{T3} in a controlled manner, Figure 4-23 (b), until the body diode of S_{T3} becomes forward biased, Figure 4-23 (c). S_{T3} is then switched on, Figure 4-23 (d), and the converter is in sub-topology (b), Figure 4-22. The inductor current increases, becoming positive again, and flows through S_{T1} , S_{T2} , S_{T3} and S_{C2} .

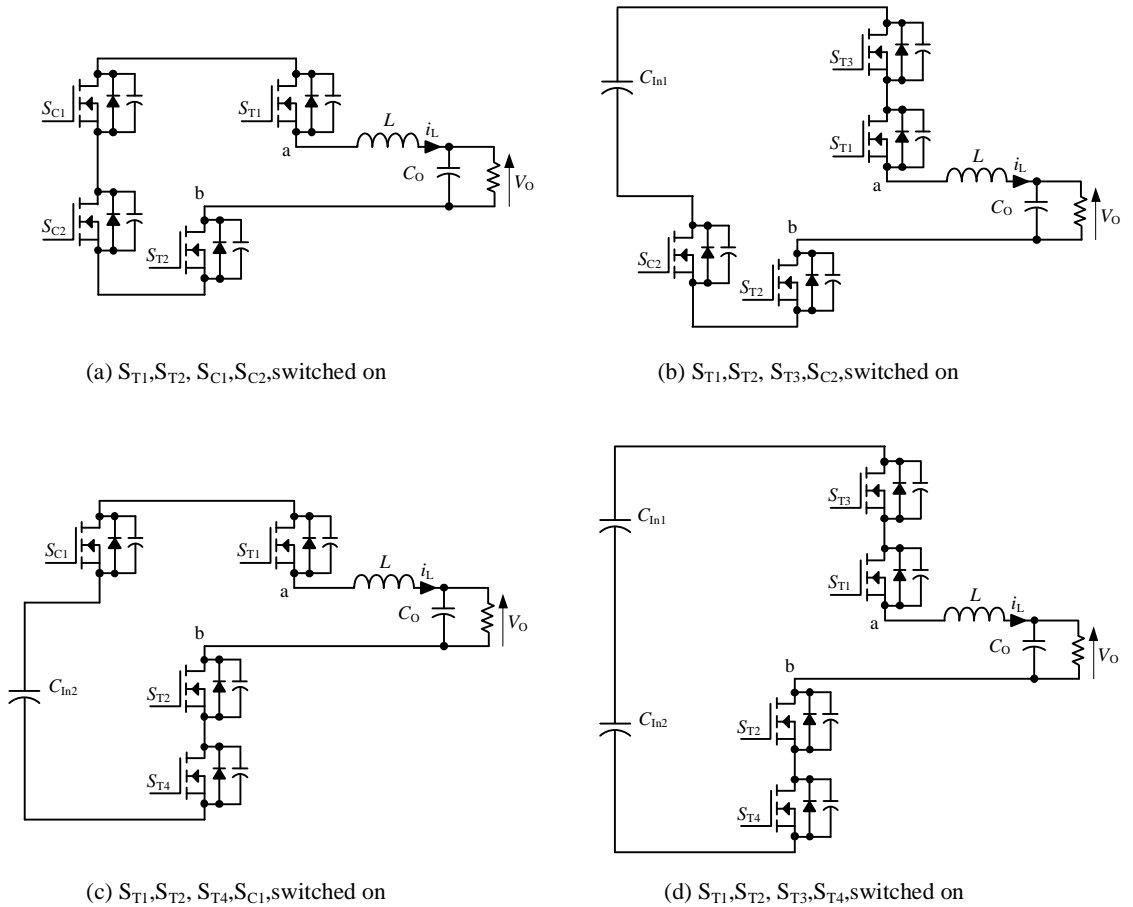


Figure 4-22 Sub-topologies for the three-level, ZVS converter operating with $D = 0.25$

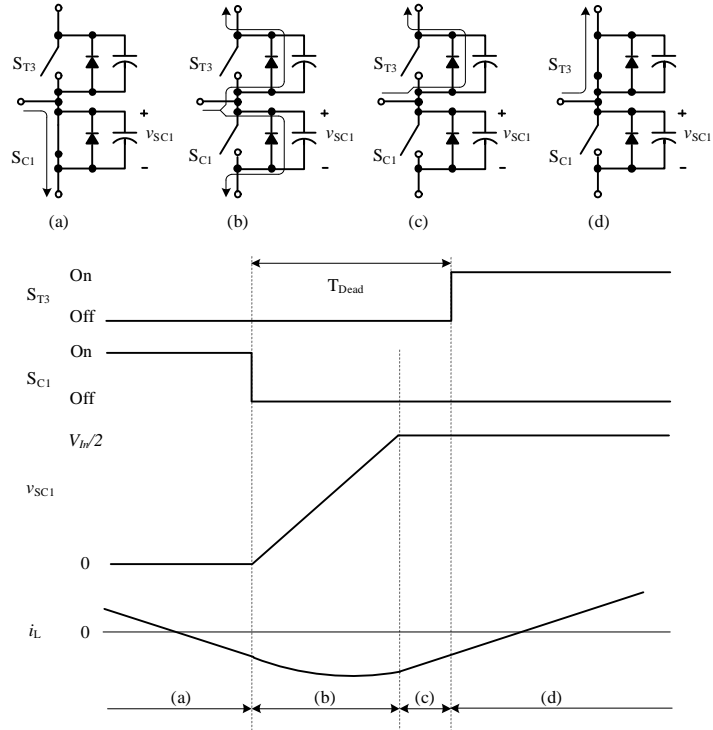


Figure 4-23 Zero-voltage commutation from S_{C1} to S_{T3}

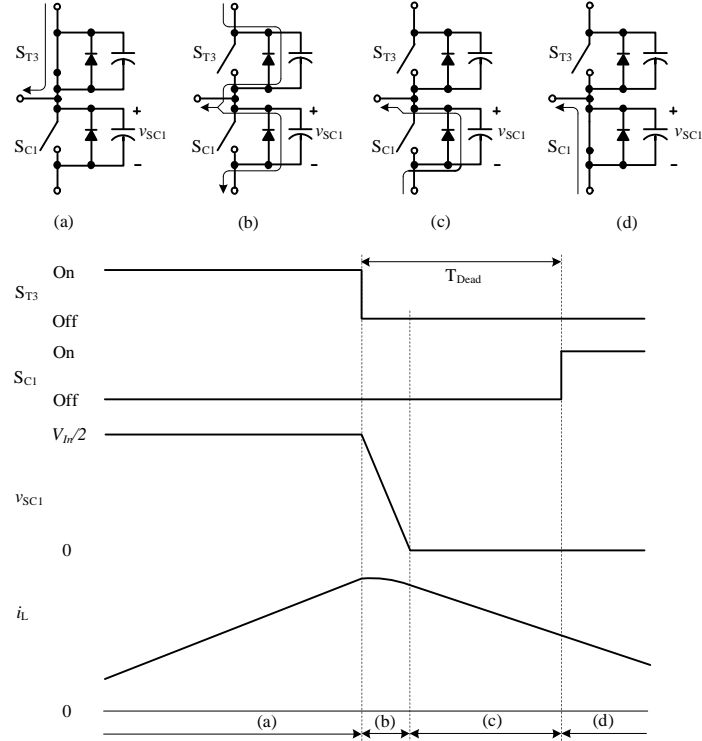


Figure 4-24 Zero-voltage commutation from S_{T3} to S_{C1}

The complementary zero-voltage-switching transient is displayed in Figure 4-24 when S_{T3} turns off. The positive inductor current charges and discharges the snubber capacitors, Figure 4-24 (b), until the body diode of S_{C1} is forward biased, Figure 4-24 (c), which allows S_{C1} to turn on at zero voltage, Figure 4-24 (d). The converter is then back in sub-topology (a), Figure 4-22.

Similarly a zero-voltage-switching transient occurs as the inductor current is commutated between S_{T4} and S_{C2} . In this way the circuit is switched into sub-topology (c), Figure 4-22, and back into sub-topology (a), Figure 4-22, in the second half of the switching cycle.

The active sub-topologies and control strategies for different ranges of positive V_o are listed in Table 4-5, in which the sub-topology letters refer to those in Figure 4-22. In each of the operating ranges listed in Table 4-5, the pair of devices that are switched are operated in an interleaved manner; the devices being switched on in alternate half cycles for an interval of DT_s , where D is the duty ratio and T_s is the period.

Table 4-5 Three-level, ZVS, one-quadrant control strategy

Operating Range	Active Subtopologies	PWM Strategies
$0 < V_o/V_{In} < 0.5$	(a), (b), (c)	S_{T1}, S_{T2} : Always On S_{T3}, S_{T4} : PWM control
$0.5 < V_o/V_{In} < 1$	(b), (c), (d)	S_{T1}, S_{T2} : Always On S_{T3}, S_{T4} : PWM control

The operation of the three-level, ZVS, step-down converter was simulated in Saber at 25 % duty ratio with a 600V supply. The value of the filter inductor was 60 μ H, and the switching frequency was 50 kHz. The resistance of the load was 37.5 Ω . Each power MOSFET was modelled by an ideal switch, an anti-parallel diode and a 0.8 nF snubber capacitor. A short dead time, 400 ns, was inserted after each MOSFET turns off in order to complete the resonant transition. All these values were calculated based on the method in Chapter 3,

Section 3.2.2 for the two-level zero-voltage-switching circuit. The simulation circuit is displayed in Figure 4-25. The schematic in Saber is shown in Appendix 7.

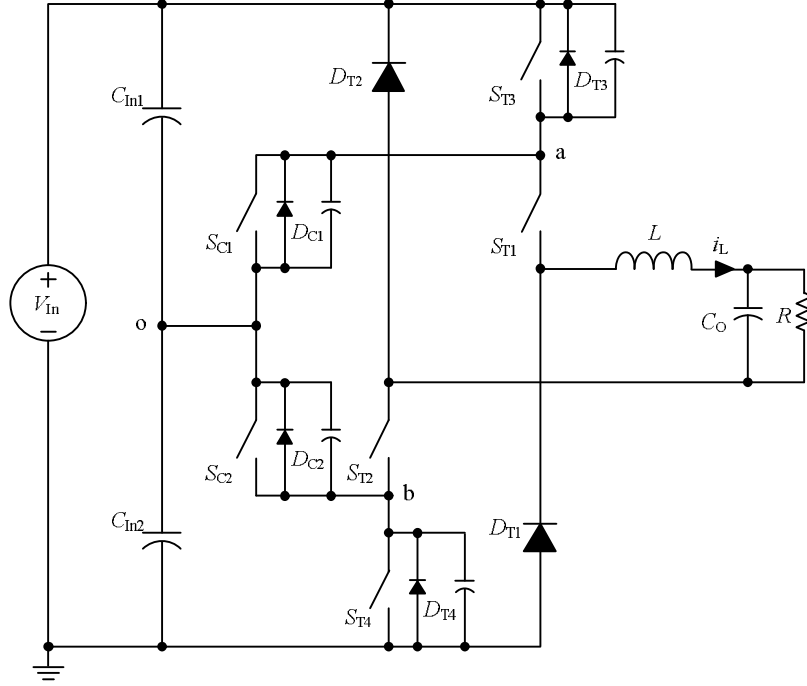


Figure 4-25 Three-level, ZVS simulation circuit in Saber operating with $D = 0.25$

The simulation waveforms are plotted in Figure 4-26 for two cycles, showing the control signals of the individual MOSFETs, the filter inductor current, the individual MOSFET anti-parallel diode currents, and the voltage and current across and through each MOSFET. The zero-voltage-switching happens in the vicinity of the maximum and minimum (negative) inductor currents, i_L . Take a pair of MOSFETs S_{C2} and S_{T4} as an example. The voltages across their snubber capacitors, v_{ob} and v_b , increase and decrease in a controlled manner, ensuring zero-voltage turn-on for each MOSFET after the body diode forward conduction, i_{DC2} and i_{DT4} in Figure 4-26. Switching losses in the three-level, ZVS converter are then virtually eliminated. Therefore, the total semiconductor loss equals the sum of the MOSFET conduction losses in (4-10).

$$P_{Semi} = P_{Conduction} = 4 \times I_{RMS}^2 R_{DS(on)} \quad (4-10)$$

where $R_{DS(on)}$ is the MOSFET on-state resistance. The total semiconductor loss in the three-level, ZVS converter operating at 25 % duty ratio is then 59.8 W at room temperature using IRFIB7N50A MOSFETs, and would decrease by a factor of eight at cryogenic temperatures according to the measured device characteristics, Figure 4-4. This value is only slightly below that measured in the practical circuits due to the much higher inductor ripple current that is required for zero-voltage-switching. The losses could be reduced by paralleling additional MOSFETs.

The three-level, ZVS, step-down converter was also simulated at duty ratios of 75 % and 50 %. The simulation schematics are displayed in Appendix 7. At 75 % duty ratio the control strategy is similar to that with 25 % duty ratio, whereas at 50 % duty ratio the MOSFETs, S_{T3} and S_{T4} , are triggered simultaneously by PWM signals, S_{C1} and S_{C2} are controlled by the complementary signals related to S_{T3} and S_{T4} . Simulation waveforms are plotted in Figures 4-27 and 4-28 respectively containing the same items and the zero-voltage-switching is achieved operating with these two duty ratios. Therefore, the semiconductor losses assuming IRFIB7N50A MOSFETs are calculated to be 6.0 W and 13.1 W at room temperature with 75 % and 50 % duty ratios respectively.

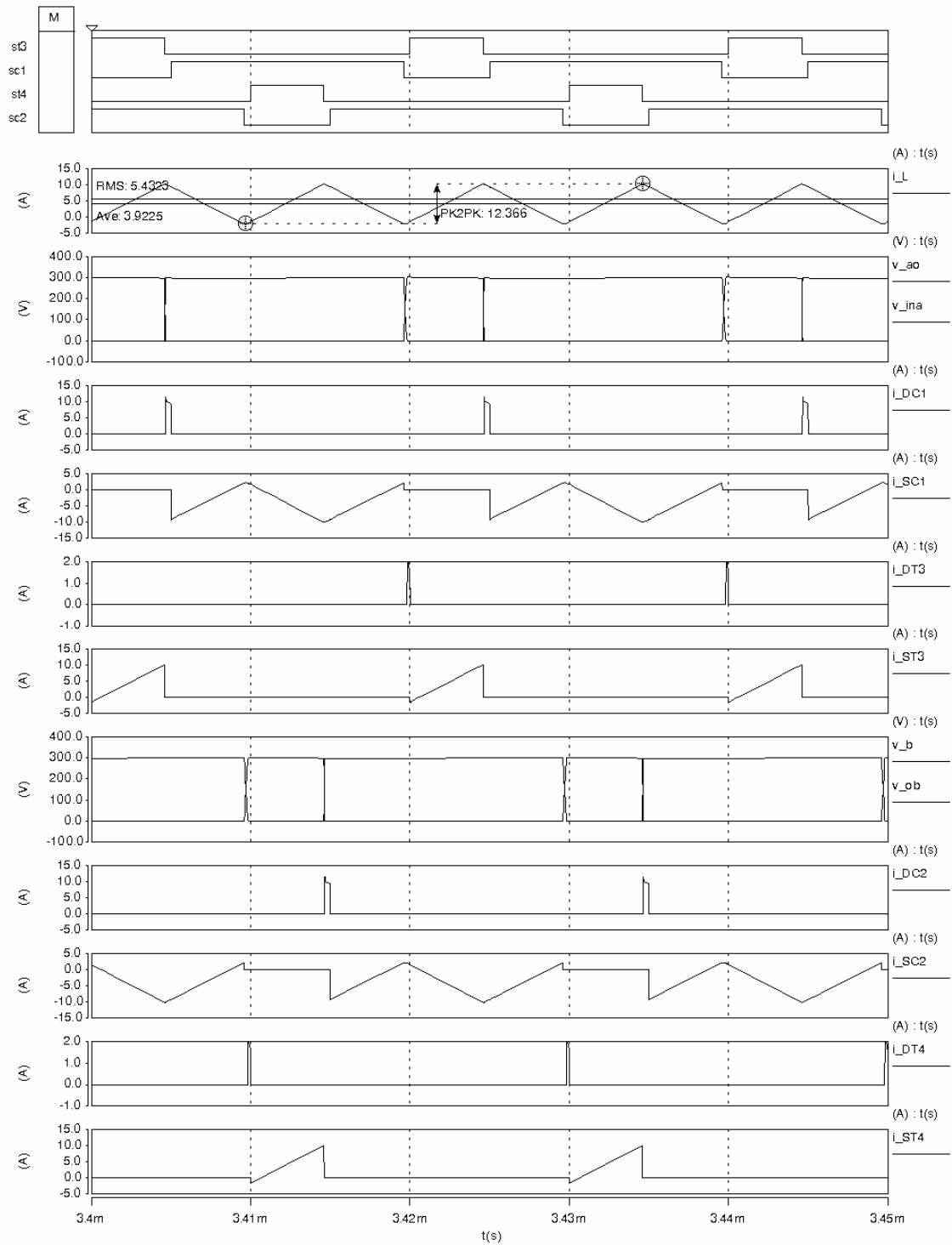


Figure 4-26 Simulation waveforms operating with $D = 0.25$

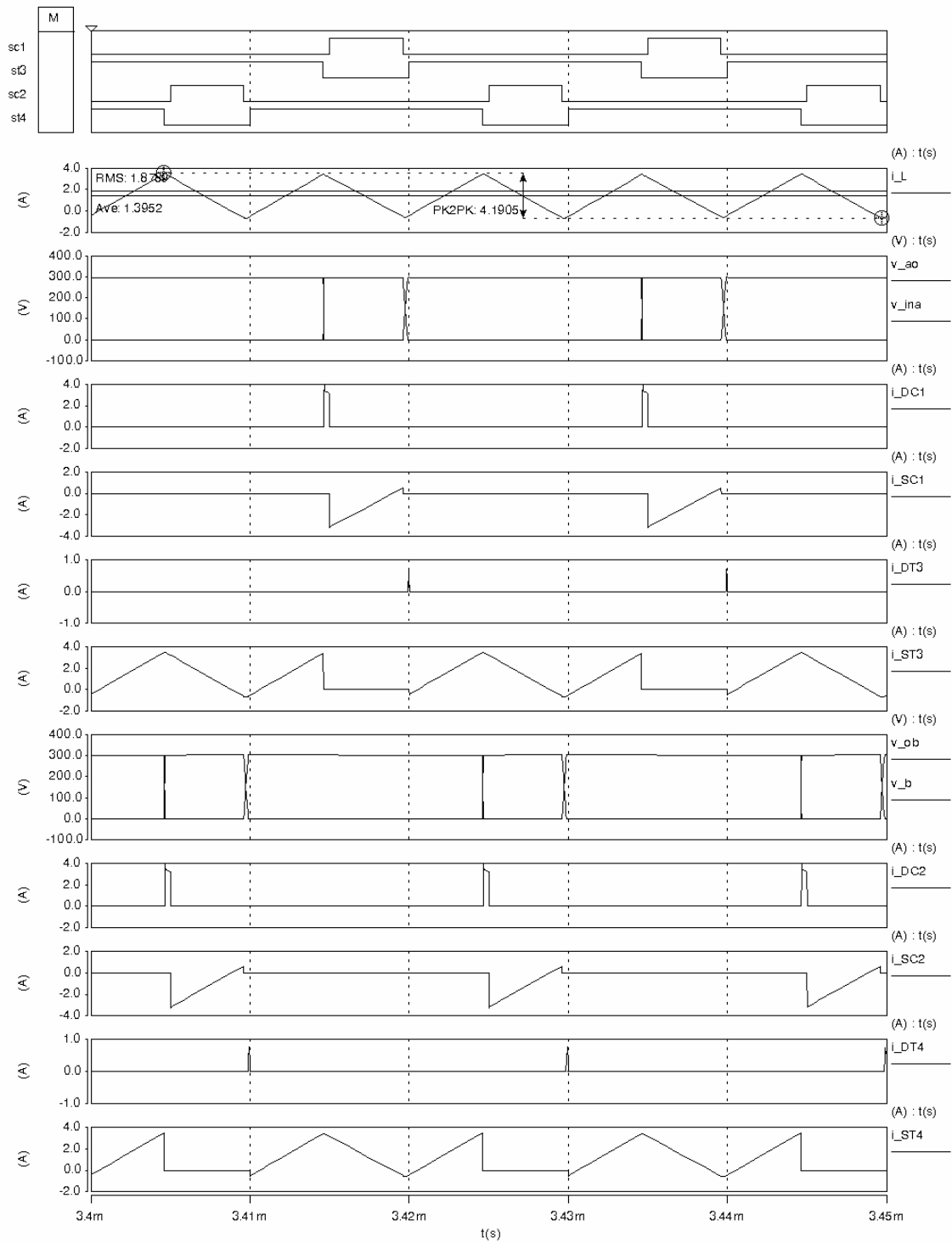


Figure 4-27 Simulation waveforms operating with $D = 0.75$

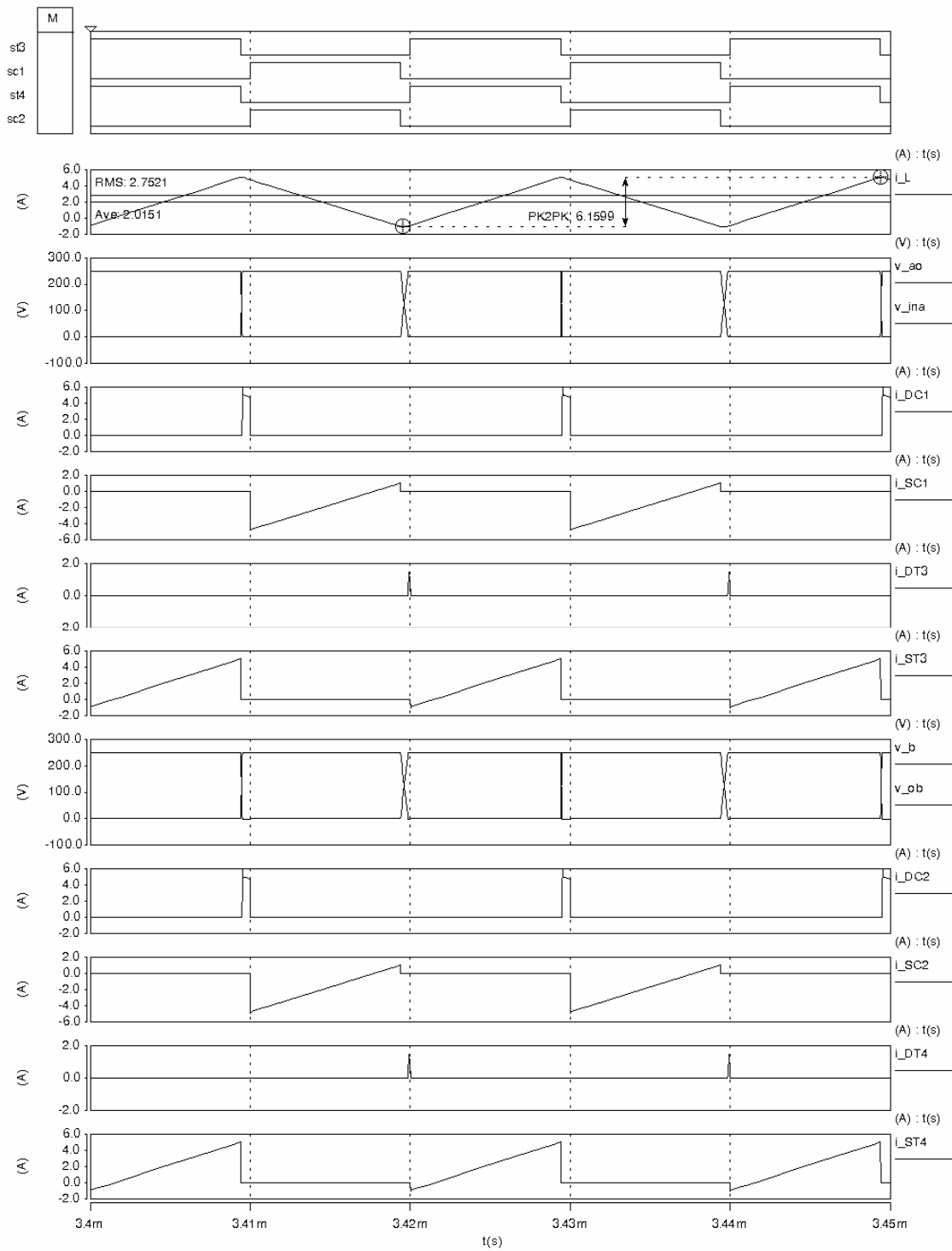


Figure 4-28 Simulation waveforms operating with $D = 0.5$

4.5 Conclusions

- All the multi-level circuits showed fairly high semiconductor losses and the losses did not exhibit such a large reduction at low temperatures as was seen for the lower voltage circuits, Chapters 2 and 3. This was due to a combination of factors, but mainly the lower current levels in the circuits, the large number of devices in the multi-level circuits, especially diodes, and the high switching losses in all circuits.
- The SiC diode based three-level converters had nearly constant switching losses, and the reduction in the total semiconductor loss at low temperature was primarily attributed to the reduced conduction loss. However, both the conduction and switching losses decreased with a decrease in temperature for the ultrafast diode based three-level converters.
- A three-level, ZVS, step-down converter was introduced to decrease the large conduction and switching losses in the three-level, diode-clamped converter. Simulation waveforms verified the operating principles at 25 %, 50 % and 75 % duty ratios.

References:

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Chapter 5

Conclusions and further work

5.1 Introduction

Advances in high temperature superconductor technology since the 1980s have stimulated the development of superconducting devices for a range of electrical power applications, such as high-voltage transmission, magnetically levitated trains, superconducting magnetic energy storage, superconducting fault current limiters and superconducting rotary machines. Many of these superconducting applications require power conditioning systems which include PWM control, AC to DC converters and DC to AC converters to interface the power at room temperature with the superconducting coils at cryogenic temperatures.

The operation of semiconductors at low temperatures offers many advantages, such as lower on-state voltages in majority carrier devices due to higher carrier mobilities, faster switching speeds in minority carrier devices due to reduced carrier lifetimes. However, on-state losses may be increased in some device types such as diodes, and freeze-out effects tend to limit device performance at extremely low temperatures. In order to understand better the performance of power electronic devices operating at low temperatures and also to identify the most appropriate circuit techniques for low temperature power conversion, this Thesis presents an experimental investigation into the performance of several DC-DC converter topologies at temperatures down to 20 K. In particular the semiconductor losses are examined in detail.

5.2 Contributions of the Thesis

The DC-DC step-down converters were built using commercial-off-the-shelf (COTS) devices, principally MOSFETs and diodes, and were mounted on a copper plate inside a cold chamber where the temperature could be controlled down to 20 K. The power losses in the semiconductors were examined over a wide range of temperatures from 300 K down to 20 K. The switching losses were calculated from measured switching waveforms, whilst the conduction losses were calculated from the measured current and static device characterisation data. The contributions of the Thesis are summarised in the following sections.

5.2.1 Device characteristics and semiconductor losses in the single-transistor step-down converters

The results from the static characterisation tests on the MOSFET and diode devices were largely consistent with the work reported in the literature; MOSFET on-state resistance fell at low temperature by up to a factor of six, the reduction being greater for higher voltage devices, however the proportionate reduction in resistance in the high voltage CoolMOS device was less than that observed in devices with a traditional structure. The diodes all exhibited an increase in on-state voltage at cryogenic temperatures at the current levels considered, the increase in the junction voltage being greater than the reduction in the voltage dropped across the drift region resistance. The breakdown voltage of all devices tested fell by around 20-24 % at cryogenic temperatures, apart from in the SiC Schottky, which showed a small increase, and this was attributed to the dominance of tunnelling breakdown in first generation of SiC diodes. The MOSFET gate threshold voltage and transconductance both increased at cryogenic temperatures; the change in threshold voltage (approximately 1 V) being quite consistent with the results reported in the literature for other

devices, however the increase in transconductance is much more device dependent, a 70 % increase was measured in this work compared with values of up to 200-300 % in some publications.

The MOSFET switching characteristics changed very little at cryogenic temperatures and this behaviour was consistent with that predicted by the standard equivalent circuit based analysis of the switching behaviour and the observed changes in threshold voltage and transconductance.

In contrast the switching behaviour of all the silicon diodes, Schottky and ultrafast, improved significantly at low temperatures, the peak reverse recovery current and reverse recovery time reduced by up to 75 % and 50 % respectively. The SiC diode showed no reverse recovery effects at any temperature.

The reduction in the total semiconductor losses in the converter prototypes at cryogenic temperatures was limited by the increase in diode conduction losses. With the duty ratio of 50 % that was used in the experimental prototypes, the total semiconductor losses fell by around 26-33 % in the low voltage, silicon diode prototypes. Using the same devices, a much greater reduction in loss would be exhibited by a converter operating at higher duty ratio due to the increased dominance of MOSFET conduction. In the higher voltage, silicon diode prototypes the reduction in loss at cryogenic temperatures was much greater, almost 50 %, due to the increased dominance of switching losses. The reduction in switching losses was almost entirely due to the improvement in diode reverse recovery at low temperatures, however, reverse recovery still remained a significant source of loss. The change in total semiconductor loss at low temperatures in the silicon carbide prototypes was very much smaller, principally due to the absence of diode reverse recovery at all temperatures. In all prototypes it was seen that switching losses and diode conduction losses were the main limitations to achieving increased conversion efficiency at cryogenic temperatures.

The prototype performance at low temperatures could be improved with a better optimised layout, in particular placing the input capacitor inside the cold chamber would allow the stray inductance and associated switching losses to be reduced.

5.2.2 Semiconductor losses in the two-transistor step-down converters

The synchronous rectifier concept was seen to work well in both the 120 V and 500 V prototypes, however to minimise the conduction of the body diode and the associated reverse recovery transient, it was necessary to optimise the dead time for each operating temperature due to the variation in gate threshold voltage with temperature. The 120 V prototype exhibited a 65 % reduction in total semiconductor losses at cryogenic temperatures, however, the efficiency at low temperature was again limited by switching losses, which varied little with temperature. The total semiconductor losses in the high voltage prototype varied little with temperature due to the dominance of switching losses.

The much lower switching losses in the zero-voltage-switching circuit allowed the overall losses to fall almost in proportion with the reduction in the MOSFET on-state resistance. The total semiconductor loss at 50 K in the zero-voltage-switching circuit was 18 % of the room temperature value and the losses could easily be reduced further by adding additional MOSFETs in parallel. Another advantage of the synchronous rectifier over the diode based circuits is that the semiconductor conduction losses will be largely independent of duty ratio for a specific output current.

5.2.3 Semiconductor losses in the three-level step-down converters

The multi-level prototypes showed fairly high semiconductor losses and the losses did not exhibit such a large reduction at low temperatures as was seen for the lower voltage circuits, which was due to a combination of factors, but mainly the lower current levels in the circuits, the large number of devices, especially diodes, and the high switching losses in all circuits. To reduce the semiconductor losses in the multi-level circuits, the synchronous rectifier and zero-voltage-switching techniques examined in Chapter 3 were successfully

applied to the circuit, resulting in a new topology that was verified by Saber simulation at 25 %, 50 % and 75 % duty ratios. Theoretically the semiconductor losses are almost entirely MOSFET conduction losses, resulting in the total semiconductor losses falling at low temperature in proportion with the reduction in MOSFET resistance.

5.3 Conclusion

It has been demonstrated that one of the most promising ways to minimise the semiconductor losses in small, cryogenic DC-DC converters is to use synchronous rectifier and zero-voltage-switching techniques. In this way the losses at cryogenic temperatures fall in proportion with the reduction in MOSFET resistance, typically being less than 20 % of the room temperature value. Further reduction in the losses could be achieved by paralleling additional devices. Furthermore, it has been shown how these techniques may be extended to multi-level topologies, allowing operation at higher voltages with low voltage MOSFETs.

5.4 Further work

Immediate further work in this area should consider the incorporation of passive devices, inductors, transformers and capacitors into the cryogenic environment and the optimum overall design of the converter.

Further characterisation and modelling of semiconductor devices are needed to underpin the design of cryogenic converters. Based on an understanding of device behaviour at cryogenic temperatures, research is needed to understand the maximum power density that can be achieved.

In the longer term, customised devices and new device materials should be investigated which may offer improved low temperature performance. Research is also required on the packaging, lifetime and reliability of devices that are operated in a cryogenic environment.

Publication

Jia, C.; Forsyth, A.J.; Evaluation of Semiconductor Losses in Cryogenic DC-DC Converters, Power Electronics and Motion Control Conference, 2006. IPEMC '06. CES/IEEE 5th International, Volume 2, 14-16 Aug. 2006, Page(s):1 - 5

Appendix 1

MOSFET gate-source voltage calculation

The detailed gate-source voltage calculation is processed by substituting (2-14) and (2-15) into (2-16) and rearranging.

$$v_{G'S'} = \frac{(V_{GH} - v_{G'S'})/(R_G + R_{G'}) - sC_{G'S'}v_{G'S'}}{sC_{G'D'}} + \frac{V_{DD} + V_F - sL_D[g_{fs} + 1/(R_G + R_{G'}) + sC_{G'S'}]v_{G'S'}}{1 + s^2L_D C_{D'S'}} \quad (A1-1)$$

Set the intermediate parameters: A , B and C

$$A = [(V_{GH} - v_{G'S'})/(R_G + R_{G'}) - sC_{G'S'}v_{G'S'}](1 + s^2L_D C_{D'S'}) \quad (A1-2)$$

$$A = \frac{V_{GH} - v_{G'S'}}{R_G + R_{G'}} - \frac{s^2L_D C_{D'S'}v_{G'S'}}{R_G + R_{G'}} - sC_{G'S'}v_{G'S'} - s^3L_D C_{D'S'}C_{G'S'}v_{G'S'} \quad (A1-3)$$

$$B = sC_{G'D'}\{V_{DD} + V_F - sL_Dv_{G'S'}[g_{fs} + 1/(R_G + R_{G'}) + sC_{G'S'}]\} \quad (A1-4)$$

$$B = -s^2L_D C_{G'D'}g_{fs}v_{G'S'} - \frac{s^2L_D C_{G'D'}v_{G'S'}}{R_G + R_{G'}} - s^3L_D C_{G'D'}C_{G'S'}v_{G'S'} \quad (A1-5)$$

$$C = sC_{G'D'}(1 + s^2L_D C_{D'S'})v_{G'S'} = sC_{G'D'}v_{G'S'} + s^3L_D C_{D'S'}C_{G'D'}v_{G'S'} \quad (A1-6)$$

Since $C = A + B$, so

$$sC_{G'D'}v_{G'S'} + s^3L_D C_{D'S'}C_{G'D'}v_{G'S'} = \frac{V_{GH} - v_{G'S'}}{R_G + R_{G'}} - \frac{s^2L_D C_{D'S'}v_{G'S'}}{R_G + R_{G'}} - sC_{G'S'}v_{G'S'} - s^3L_D C_{D'S'}C_{G'S'}v_{G'S'}$$

$$-s^2 L_D C_{G'D'} g_{fs} v_{G'S'} - \frac{s^2 L_D C_{G'D'} v_{G'S'}}{R_G + R_{G'}} - s^3 L_D C_{G'D'} C_{G'S'} v_{G'S'} \quad (A1-7)$$

Rearranging the above equation (A1-7) gives

$$V_{GH} = v_{G'S'} [s^3 L_D (R_G + R_{G'}) (C_{G'D'} C_{G'S'} + C_{D'S'} C_{G'S'} + C_{D'S'} C_{G'D'}) + s^2 L_D \{C_{D'S'} + C_{G'D'} [1 + g_{fs} (R_G + R_{G'})]\} + s (R_G + R_{G'}) (C_{G'D'} + C_{G'S'}) + 1] \quad (A1-8)$$

Set the following time constants to simplify the calculation.

$$t_{G3}^3 = L_D (R_G + R_{G'}) (C_{G'D'} C_{G'S'} + C_{G'S'} C_{D'S'} + C_{D'S'} C_{G'D'}) \quad (A1-9)$$

$$t_{G2}^2 = L_D \{C_{D'S'} + C_{G'D'} [1 + g_{fs} (R_G + R_{G'})]\} \quad (A1-10)$$

$$t_G = (R_G + R_{G'}) (C_{G'D'} + C_{G'S'}) \quad (A1-11)$$

Therefore, the gate-source voltage expression is simplified to

$$v_{G'S'} = \frac{V_{GH}}{s^3 t_{G3}^3 + s^2 t_{G2}^2 + s t_G + 1} \quad (A1-12)$$

Considering the source stray inductance L_S , the gate-source voltage expression is simplified to the following equation [A1-1].

$$v_{G'S'} = \frac{V_{GH}}{s^2 t_m t_{G'} + s(t_G + L_S g_{fs}) + 1} \quad (A1-13)$$

where

$$t_{m'} = g_{fs}(L_D + L_S) \quad (\text{A1-14})$$

$$t_{G'} = C_{G'D'}(R_G + R_{G'}) \quad (\text{A1-15})$$

$$t_G = (R_G + R_{G'})(C_{G'D'} + C_{G'S'}) \quad (\text{A1-16})$$

The drain-source voltage in (2-21) and (2-36) is recalculated considering the source stray inductance L_S [A1-1, A1-2].

$$v_{D'S'} = V_{DD} + V_F - g_{fs}(L_D + L_S)(V_{GH} - V_T) \frac{\exp(-t/t_b) - \exp(-t/t_c)}{t_b - t_c} \quad (\text{A1-17})$$

$$v_{D'S'} = V_{DD} + V_F + (L_D + L_S)(g_{fs}V_T + I_O) \frac{\exp(-t/t_b) - \exp(-t/t_c)}{t_b - t_c} \quad (\text{A-18})$$

Reference:

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Appendix 2

Temperature control circuit

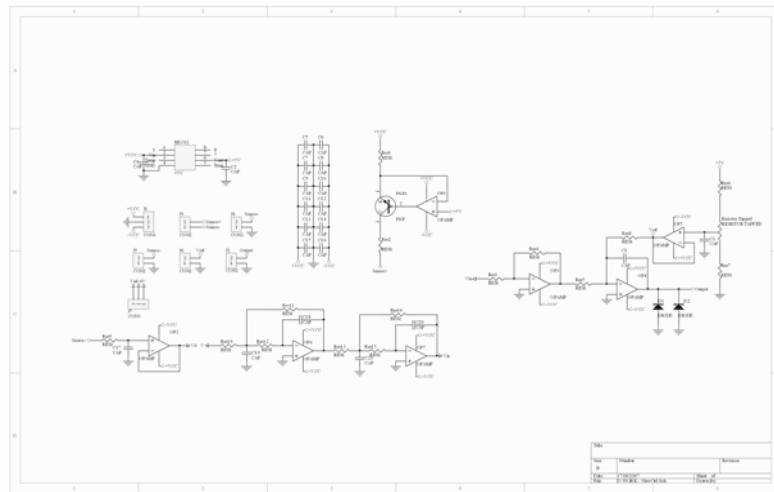


Figure A2-1 Schematic diagram of the temperature control circuit

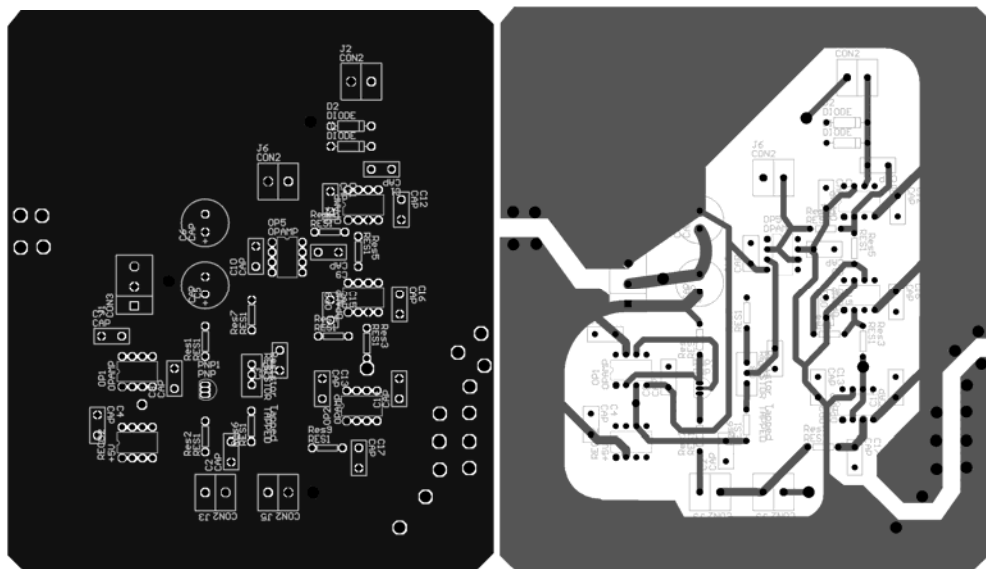


Figure A2-2 PCB design of the temperature control circuit (zoom out): top layer (left) and bottom layer (right)

Appendix 3

Cryogenic experimental system



Figure A3-1 Overview of the cryogenic experimental system

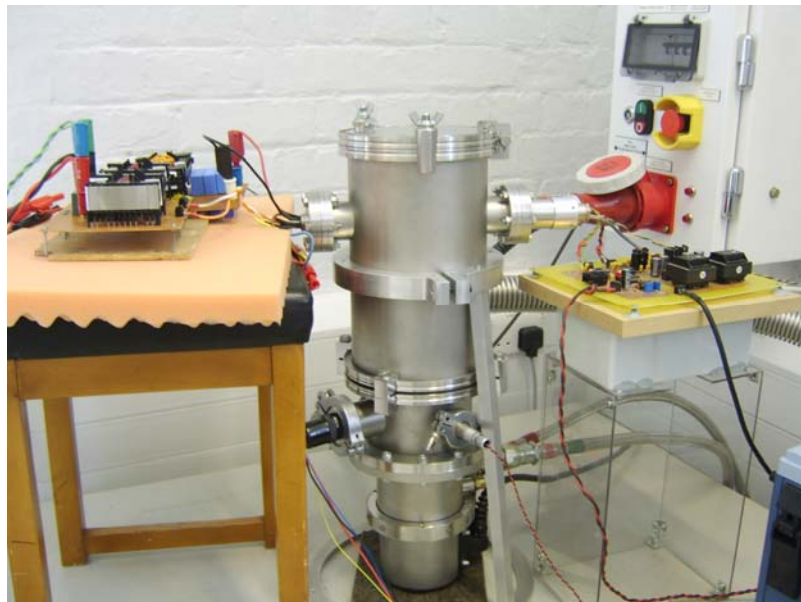


Figure A3-2 Experimental layout



Figure A3-3 Cold chamber and compressor

Appendix 4

Cryogenic test circuits for single device characteristics

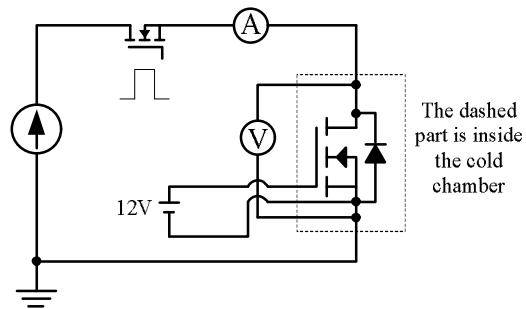


Figure A4-1 Test circuit for MOSFET on-state resistance

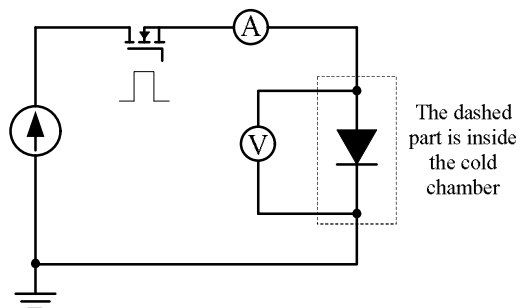


Figure A4-2 Test circuit for diode on-state voltage

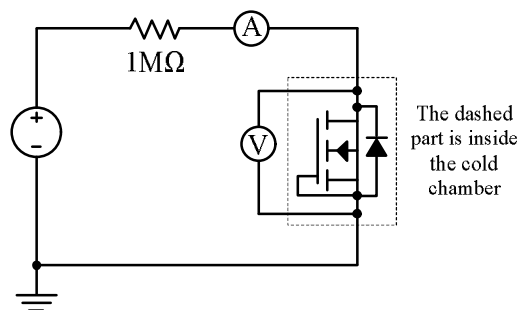


Figure A4-3 Test circuit for MOSFET breakdown voltage

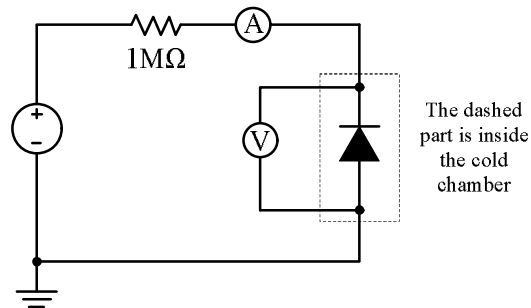


Figure A4-4 Test circuit for diode breakdown voltage

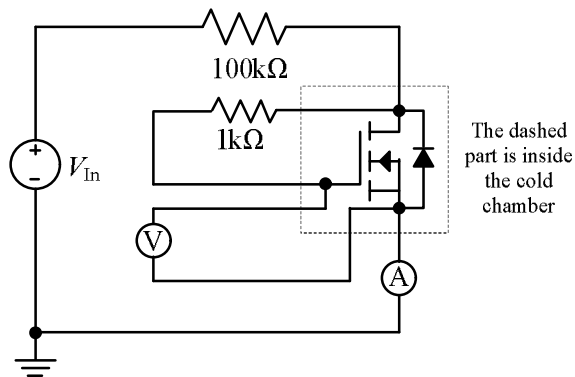


Figure A4-5 Test circuit for MOSFET threshold voltage

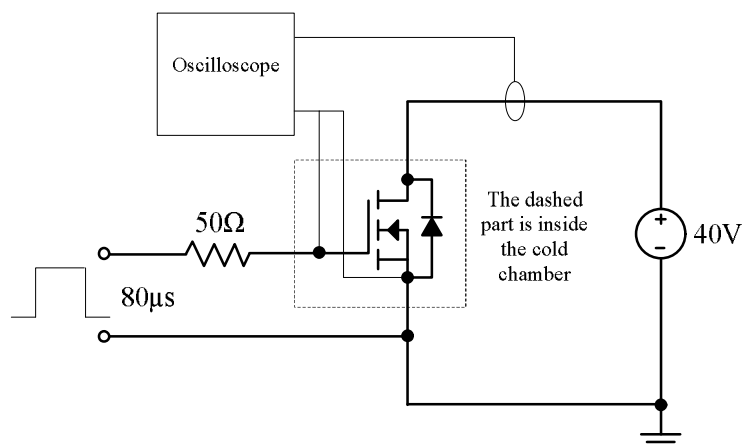


Figure A4-6 Test circuit for MOSFET transconductance

Appendix 5

Power conversion circuits inside cold chamber

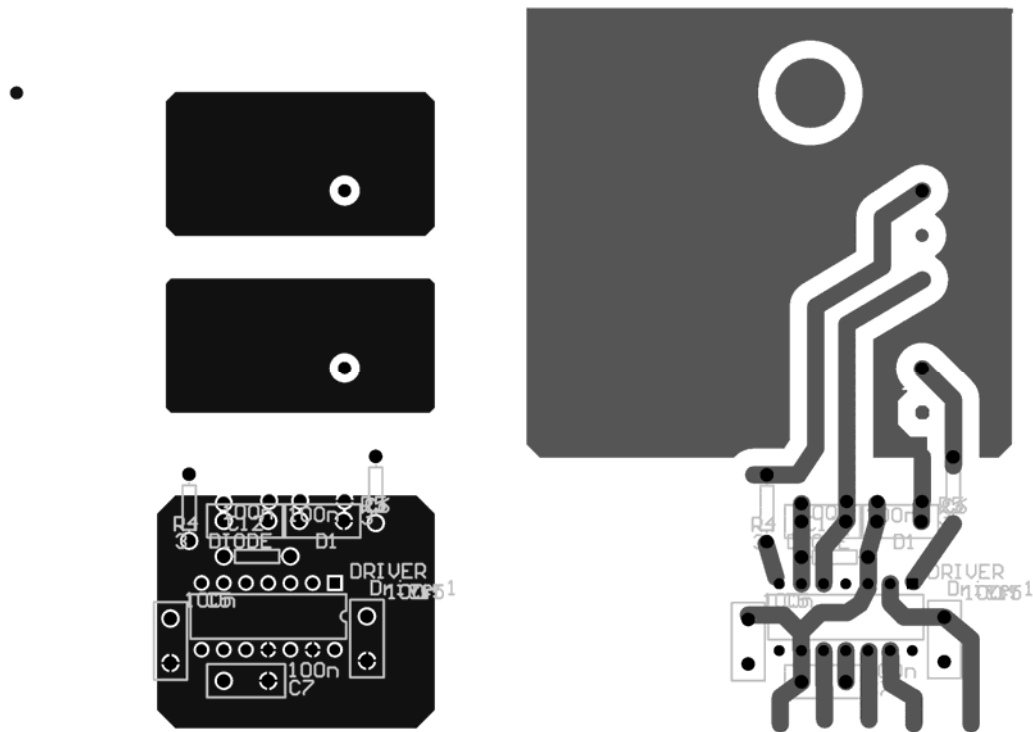


Figure A5-1 PCB design of the step-down conversion circuit (zoom out): top layer (left) and bottom layer (right)

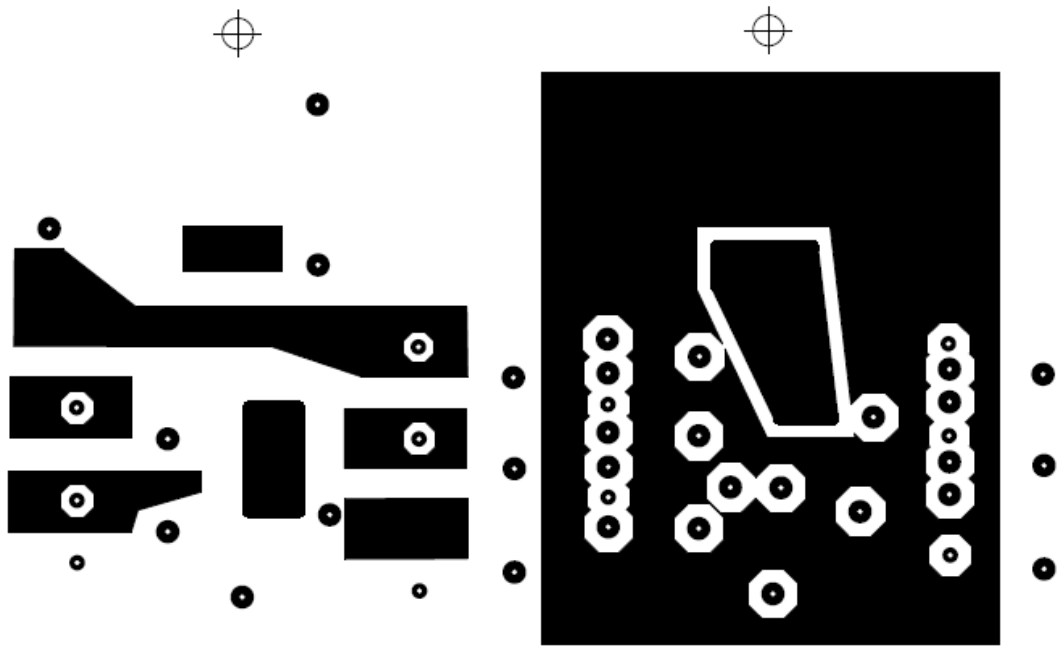


Figure A5-2 PCB design of the three-level, diode-clamped conversion circuit (zoom out): top layer (left) and bottom layer (right)

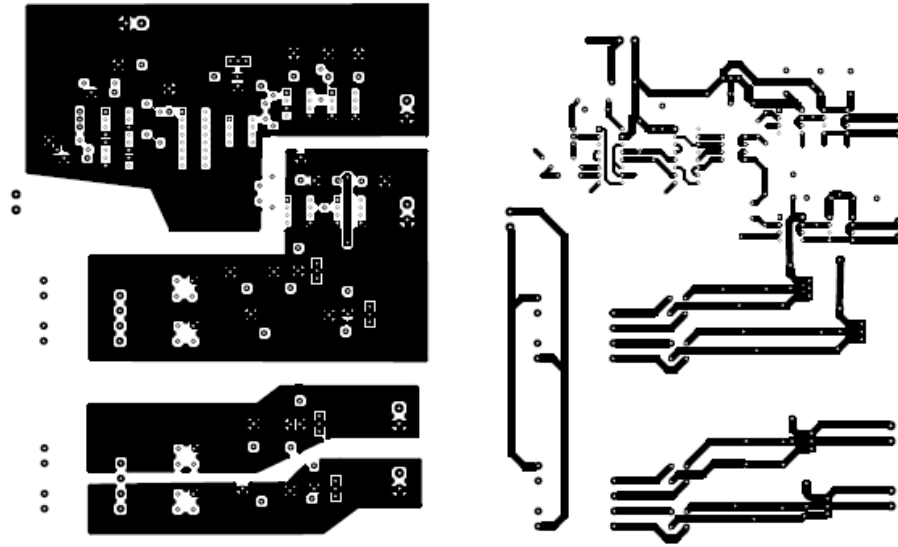


Figure A6-2 PCB design of the three-level converter control circuit (zoom out): top layer (left) and bottom layer (right)

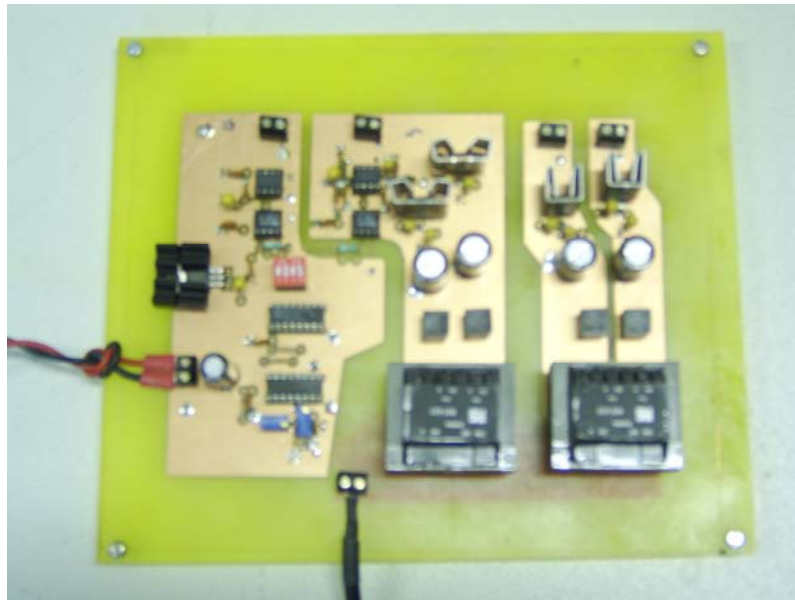


Figure A6-3 Photograph of the three-level converter control circuit

Appendix 7

Three-level ZVS converter simulation schematics

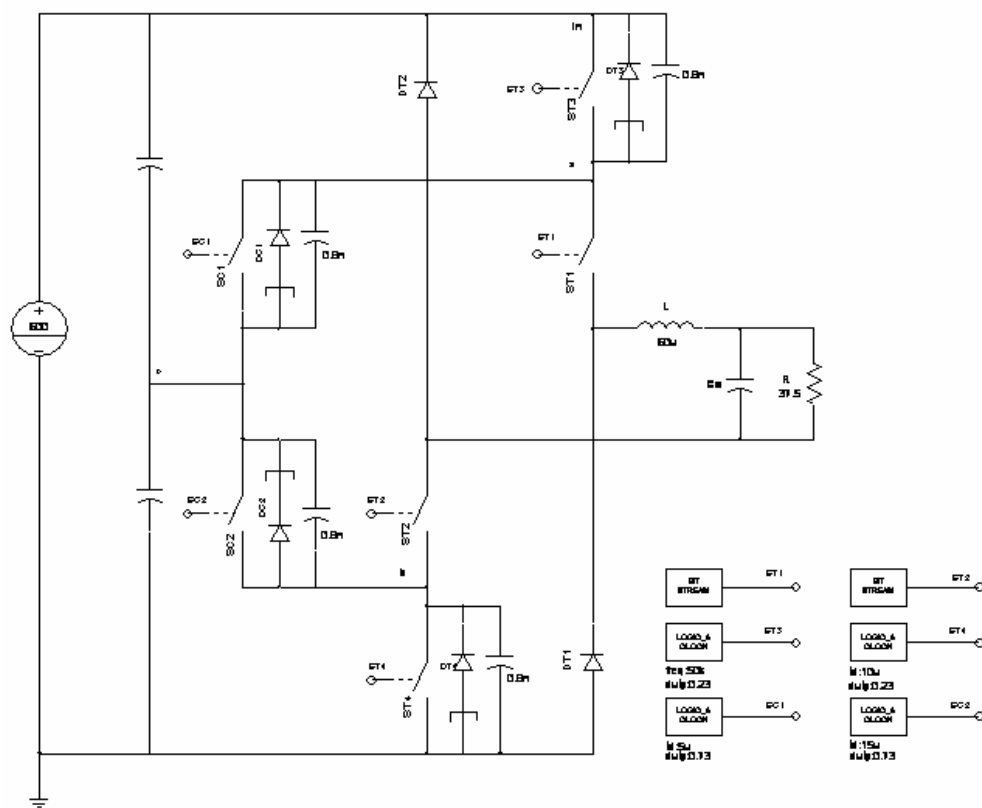


Figure A7-1 Three-level, ZVS converter simulation circuit at 25 % duty ratio in Saber

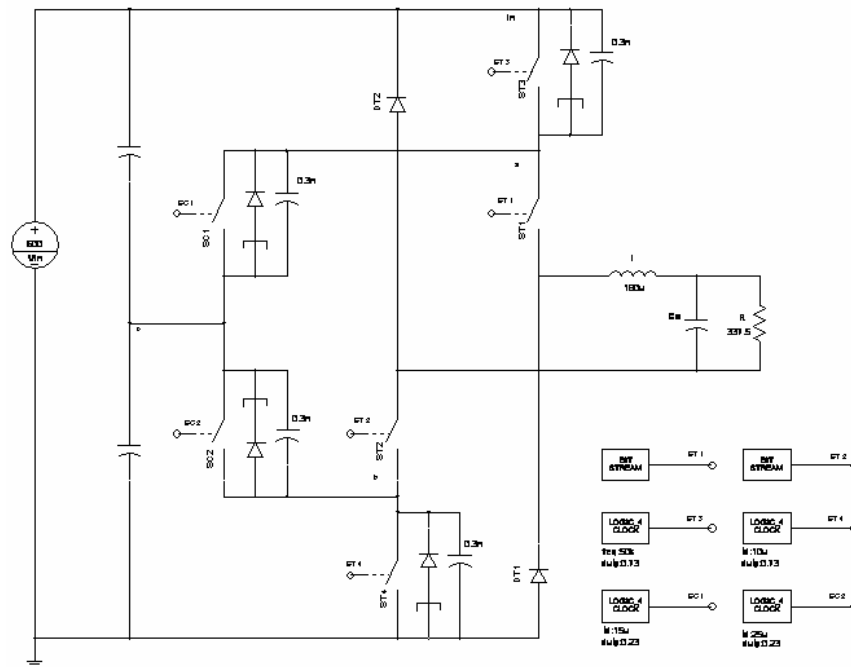


Figure A7-2 Three-level, ZVS converter simulation circuit at 75 % duty ratio in Saber

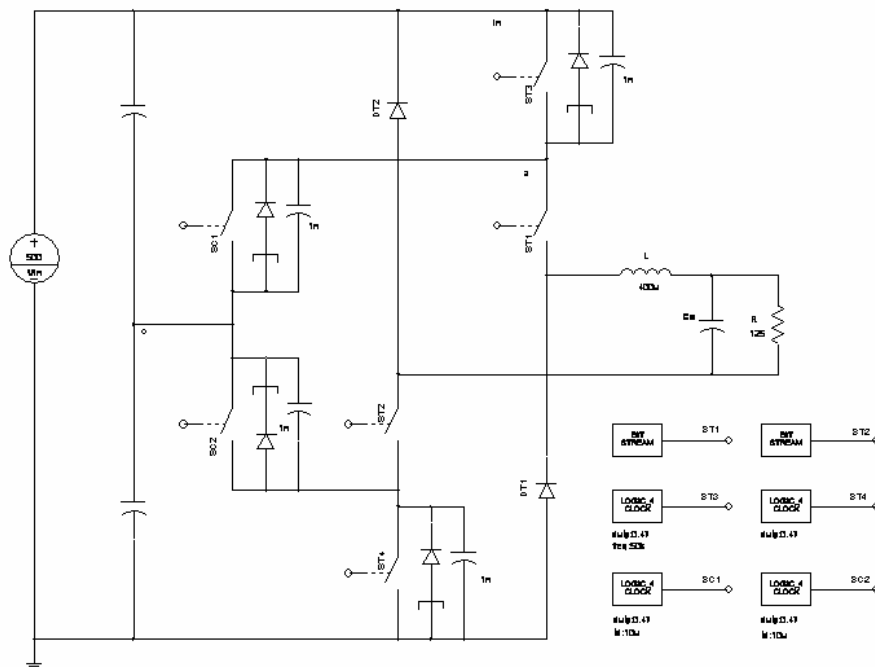


Figure A7-3 Three-level, ZVS converter simulation circuit at 50 % duty ratio in Saber